OPERATION AND SERVICE MANUAL FOR RADIO DIRECTION FINDERS DDF-4001, 4002, 4003 AND 4004

DOPPLER SYSTEMS, INC.

LIMITED WARRANTY INFORMATION

Doppler Systems, Inc. will repair or replace, at our option, any parts found to be defective in either materials or workmanship for a period of one year from the date of shipping. Defective parts must be returned for replacement. Contact the factory before returning any equipment for instructions.

If a defective part or design error causes your Radio Direction Finder to operate improperly during the one year warranty period, Doppler Systems, Inc. will service it free of charge if returned at owner's expense. If improper operation is due to an error on the part of the purchaser, there will be a repair charge.

Doppler Systems, Inc. is not responsible for damage caused by the use of improper tools or solder, failure to follow the printed instructions, misuse or abuse, unauthorized modifications, misapplication of the unit, theft, fire or accidents. This warranty applies only to the equipment sold by Doppler Systems, Inc. and does not cover incidental or consequential damages.

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SECTION 1.0
INTRODUCTION

The radio direction finding system you have purchased adds modern quasi-Doppler direction finding capability to your VHF or UHF narrow band FM receiver. Radio direction finders based on the Doppler principle have been used in aeronautical applications for many years. While their performance is generally much better than other methods of direction finding, conventional Doppler-type systems have been large, complex and expensive. In a typical system, an array of eight to sixteen antennas is switched electronically to approximate a single rotating antenna. The patented principle on which your radio direction finder works simulates a smoothly rotating antenna by continuously summing the outputs of four antennas mounted in a square array. As the simulated rotating antenna moves toward the RF source, an increase in the apparent signal frequency occurs, and as the antenna recedes from the source, this frequency decreases. This up-down (Doppler) shift is detected by your FM receiver and is present as a 300 Hz tone on the audio output. Since the phase of this tone is related to the bearing angle, your direction finder electronics can compute and display the bearing information without any modification to your receiver.

A directional gain is also formed by the interaction of currents in the four antennas which produces a 300 Hz amplitude modulation of the signal at the same time that it is phase modulated as described above. This allows the system to be used with an AM receiver to direction find signals in the aircraft band, such as Emergency Locator Transmitters (ELT's).

Four models of direction finders are covered by the manual. Model DDF4001 displays the bearing angle with 16 high intensity LEDs arranged in a circular pattern. DDF4002 displays the bearing directly in degrees (3 digits) as well as in a circular array. Model DDF4003 has a display identical to the DDF4002, and it provides an RS232C output of the 3 digit bearing angle for computer analysis, triangulation, data logging, etc. Model DDF4004 also has a display identical to the DDF4002, and it contains a speech synthesizer, audio amplifier and loudspeaker to enunciate the bearing angle. This model is designed for mobile use, as it eliminates the need for the driver to watch the display. An external audio output permits unattended or remote operation using a tape recorder, telephone or repeater link.

This manual contains instructions for installing, adjusting and using your direction finder. A troubleshooting section and detailed technical description are included which should cover most service situations.

You have purchased an instrument which has been designed to give you trouble-free, accurate radio direction finding. Be sure to read the installation and adjustment instructions thoroughly and follow all of the directions carefully to avoid unnecessary problems.

SECTION 2.0
INSTALLATION AND ADJUSTMENT

2.1 ANTENNAS

Proper operation of your radio direction finder requires care in the construction and installation of the antenna system. The most important consideration is to maintain symmetry in the system. Each of the four antennas used must be electrically identical. Either quarter wave whips or gain types may be used, but the phase shifts (i.e., impedances) of all four must be the same. For this reason, it is generally easier to use quarter wave whips. Be sure to cut the whips to resonance using the cutting chart supplied.

Both fixed and mobile antennas which are available from Doppler Systems have the required equal length of coax. If you are making your own, be certain that the feed lines of all four antennas have the same **electrical** length. It is best to cut all coax used from the same spool and to match line lengths within 1/4 inch. Apply equal tension to the feedlines when measuring and cutting. RG58A/U is recommended. Place cable markers A, B, C and D at each end for ease in installation and phasing. Install BNC plugs on the direction finder end.

A good choice of antenna for mobile use is four magnetic mounts with removable whips. This permits using your direction finder on several frequencies by simply changing the antenna spacing and whip length. Place the antennas in a square pattern in the center of your car's roof with antenna A at the left front, B at the left back, C at the right back and D at the right front. Space the antennas with about 3/16th wavelength between adjacent antennas. (One of the whips may be marked to make a convenient measuring rod.) The spacing is not critical and can be varied from 1/8th to 1/4th wavelength. Regardless of the size, be sure that the four antennas form a **square** pattern and that a reasonable ground plane will exist under each. (Don't place the four antennas close to the edge of the roof.)

It is a good idea to remove any other antenna from the car when using the direction finder. If you must use another antenna, try to mount it well below the direction finder array or alternatively mount it in the exact center of the square array. **Do not transmit more than a few watts in the immediate vicinity of the direction finder antenna - especially in the same frequency band for which the direction finder antennas are cut.** The direction finder may be damaged if more than 100 milliwatts are induced into its input.

Fixed station antennas can be fabricated using an aluminum X-frame to support the four elements and form a ground plane. Element spacing should be between 1/8th and 1/4th wavelength. Mount the array well above or away from other radiating antennas or structures. A side arm mount on a tower would be a very poor choice. A better design would be at the top of a separate mast near the direction finding unit and away from the tower. Cable length should be kept reasonably short to minimize line loss.

2.2 RECEIVER

A narrow band FM receiver is required to detect the phase modulation produced by the mixing of the four antenna signals in the RF section of the direction finder. You can also track AM signals with the receiver in the narrow band FM mode.

NEVER TRANSMIT INTO THE DIRECTION FINDING UNIT! If you plan to use a transceiver for the receiver, disconnect the microphone or otherwise disable the unit from transmitting with the direction finder connected.

For best performance, a dedicated receiver tuned to the band of interest gives best performance. Scanner receivers are very convenient, but the poor intermod characteristics of some of the cheaper units may limit their usefulness in many locations. Also, a few of the scanners currently on the market are not designed to provide audio output at 300 Hz. This problem can generally be corrected by increasing the audio coupling capacitor(s).

Connect the receiver to the direction finder as shown in Figure 2-1. The external speaker jack should be rewired if necessary so the internal speaker is not cut off. Alternatively, an external speaker may be paralleled with the direction finder audio input (pin 8 high, pin 7 ground on the 15 pin subminiature D connector). Use a **small** shielded wire for the audio input.

2.3 POWER

Connect the direction finder to a source of +12 VDC power. Use number 20 or 22 size wire and connect to pin 15 (high) and pin 13 (power ground) on the 15 pin connector. Connect the power and power ground wires from the direction finder and the receiver separately to the power source (dc supply, cigarette lighter, etc.) rather than daisy chaining them together. In some vehicles, an in-line noise filter may also be needed.

The direction finder is internally fused at 2 amperes, but draws less than 0.5 amperes. A 1 ampere in-line fuse can be used if desired.

2.4 CALIBRATION

Tune the receiver to the frequency of a known signal, such as a NOAA weather station or a local repeater. Adjust the bearing calibration pot on the back of the unit until the correct bearing is displayed. For mobile use the bearing is calibrated relative to the car -- that is, 0 degrees is straight ahead, 90 degrees is right, etc. In fixed operation, 0 degrees should be due North, 90 degrees East, etc.

If the correct bearing cannot be obtained by adjusting the pot, rotate the antenna itself or rotate the antenna leads at the BNC

connectors so that the system will calibrate with the control near the center of its range. Be sure not change the order of rotation of the four antennas, however.

Generally, the calibration is not affected when changing frequencies within a given band. If the receiver, antenna or band are changed (for example, from high band VHF to UHF), you should recalibrate on a known signal.

Check the calibration and operation of the system in a vehicle by driving in a circle while monitoring the known station. Choose a location free of reflections when calibrating a mobile unit. A large empty parking lot away from power lines, buildings, etc. would be ideal.

2.5 OPERATION

Bear in mind that an ideal direction finder will indicate the angle of arrival of the incoming wave front. If the direct path between the transmitter and receiver is blocked, your direction finder is likely to point toward a reflection. The only method of eliminating this problem is by locating the direction finder where a direct path exists. In mobile use, it is sometimes better to drive to a clear high location such as a hilltop or the top floor of a multi-story parking lot in order to get a good "initial bearing." As you drive closer to the transmitter, the bearing direction will become more stable.

When both a direct and reflected signal are received (multi-path), your direction finder will also give an erroneous indication. However, if you listen closely to the sound of the 300 Hz tone in the receiver audio, you will notice that it sounds "raspy" on a multipath signal and is a purer tone on a direct signal. With practice, this can be an important clue in knowing when to believe the readings. Frequently driving forward a few feet can eliminate the multipath.

Modulation on the transmitted signal will cause the bearing display to vary a few degrees. This effect is usually not important as it averages out.

2.6 OPTIONAL CONNECTIONS

Your direction finder contains an automatic level control circuit that adjusts to changes in the audio output level from the receiver. When no output is present, that is, when the receiver is squelched, the display will hold for about 6.8 seconds, then automatically blank. If you want to have the display hold indefinitely, move the shorting plug at J9 connecting pins 2 to 3 and reinsert it to short pins 1 and 2.

As supplied, the direction finder display is synchronized to the audio signal from the receiver and will operate with transmitted pulses of 150 milliseconds or longer. If your receiver provides a "mute" signal of 5 to 9 VDC, it may be connected to pin 14 of the

15 pin connector. Remove the shorting plug at J8 connecting pins 2 and 3 and reinsert it to short pins 1 and 2 to use the external mute signal.

2.7 MOUNTING

A bracket is provided for mounting your direction finder below the dash in your car. In very hot weather, however, locate or cover the direction finder so that it is not in the direct sun with the car closed for an extended period. **The enclosure can distort if heated above 150 degrees F (65 degrees C).**

2.8 SERIAL INTERFACE CONNECTIONS (Model DDF4003)

The serial output for connection to a digital computer is shown in Figure 2-2. Keep the cable length under 50 feet. A shielded cable is recommended. Set the computer to 300 Baud and match the number of data bits and parity of the direction finder to that at the computer. The following switches are located inside the direction finder on the Serial Interface board.

Switch	OFF	ON
SW1-1	No parity bit	Parity bit
SW1-2	8 data bits	7 data bits
SW1-3	Even parity	Odd parity

2.9 SYNTHESIZED SPEECH CONNECTIONS (Model DDF4004)

A constant level output is available on this model for connection to an acoustical coupler as shown in Figure 2-3 for remote telephone monitoring. The same output may also be connected to the audio input on a tape recorder for unattended monitoring or to a down link radio channel for remote use.

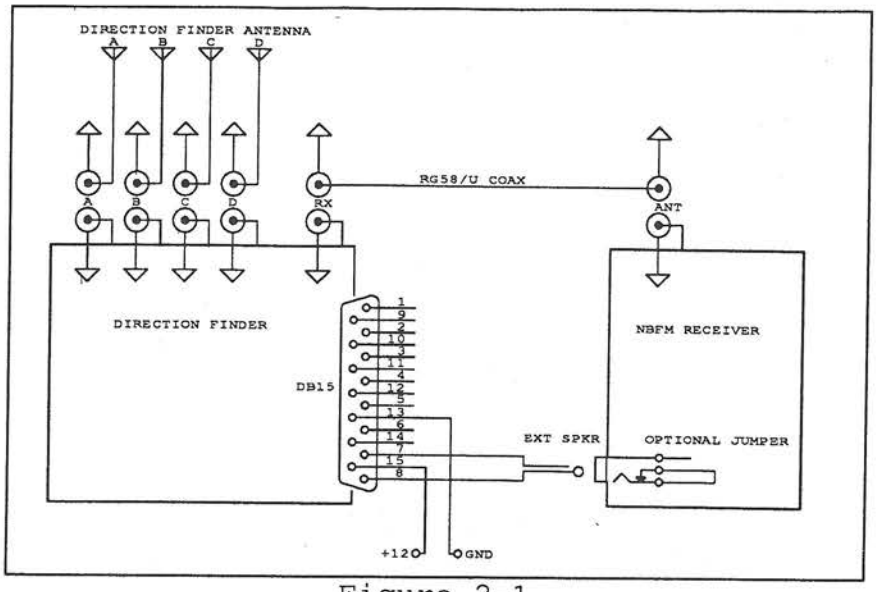


Figure 2-1
Direction Finder Connections (All Models)

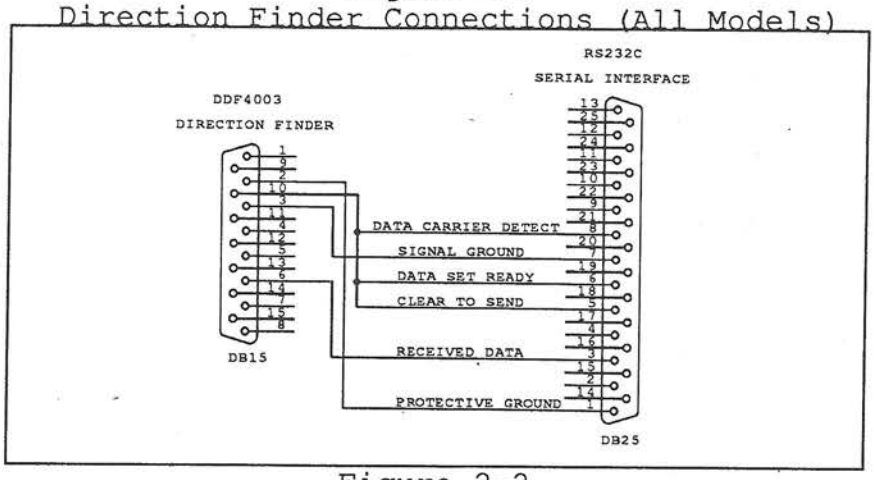


Figure 2-2
Serial Interface Connections (Model DDF4003)

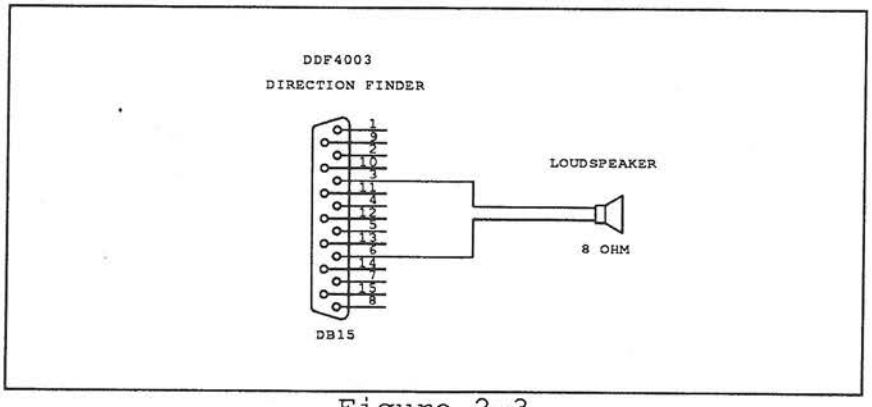


Figure 2-3
Synthesized Speech Connections (Model DDF4004)

SECTION 3.0
CHECKOUT AND TROUBLESHOOTING

Follow the procedure below if your direction finder does not appear to be operating correctly. If a problem is found, refer to the detailed technical description and circuit schematics given in Section 4.0 to isolate the problem or return your unit to Doppler Systems Inc. for servicing.

With the direction finder connected normally, verify that a 300 Hz tone is audible in the receiver with a strong signal tuned in. If no tone is heard, the problem may be in the RF summer. If your receiver has an S-meter, you can make a coarse test of the RF summer by connecting only one antenna to an input and noting the "S" reading. Connect the same antenna to the other three inputs and see whether the same reading results. All four readings should be approximately equal.

If the display unit itself does not appear to be operating correctly, perform the following simple self test. Connect a short jumper wire between pins 1 and 8 on the 15 pin cable connector. (Disconnect pin 8 from the receiver if it was previously installed.) Connect +12 VDC to pin 15 and power ground to pin 13 as shown in Figure 3.1-1. There should be no other connections to the unit for these checks.

Turn the set on. The power light should light and a bearing should be displayed.

After a few seconds, the display should settle out to a steady value. Check that the brightness control operates properly. Adjust the bearing calibration on the back panel and verify that the display changes. If you have a model DDF4004, check that the volume control functions correctly. The circular display, 3 digit readout and synthesized voice output should all agree.

The above tests verify practically all of the circuitry in your unit, and it is not necessary to proceed with the remaining checks in this section unless you suspect there is a problem. If you do not need to continue with a detailed checkout, remove the jumper wire between connector pins 1 and 8 and reconnect the unit to your receiver as described in Section 2.

To perform a detailed checkout, place a soft cloth on your work table and remove the four screws which hold the upper and lower halves of the enclosure together. Slide the upper half of the box straight up off the front panel and set it upside down next to the bottom half. You do not need to remove any of the printed circuit boards from the unit to make the measurements below.

A good dc oscilloscope is required to check the following voltages and waveforms. The scope probe should have a straight point and the scope ground should be connected using a miniclip to the center lead on the +5 VDC regulator (U1) which is mounted flat against the heat sink on the Processor board. This is the large printed wiring

board mounted on the floor of the bottom half of the enclosure. Be sure that the scope ground clip does not short against the other pins on the IC.

3.1 PROCESSOR BOARD CHECKOUT

Measure the voltage at U4, pin 16. It should be +5.0, +/-0.25 VDC.
Measure the voltage at U6, pin 14. It should be +9.0, +/- 0.5 VDC.
Measure the voltage at U20, pin 5. It should be +4.5, +/-0.25 VDC.

Observe the 1.728 MHz clock waveform on U6, pin 3. It should appear similar to Figure 3.1-2.

Observe the 38400 Hz waveform at U12, pin 15. With the scope set for 2 V/div and 5 microseconds/div, it should appear similar to Figure 3.1-3.

Check the following additional clock waveforms. These should all be 8 to 9 volt peak to peak square waves having the periods listed below:

Signal	Location	Period
108000	U10, pin 6	9.26 microseconds
2400	U18, pin 6	417 microseconds
300	U18, pin 13	3.33 milliseconds
18.75	U10, pin 13	53.3 milliseconds

Check the master reset (MR) waveform at U16, pin 1. With the scope set for 2 V/div and 1 microsecond/div, it should appear similar to Figure 3.1-4.

All four RF summer control voltages should appear as 300 Hz sinusoids, approximately 3 V peak to peak, offset by 4.5 VDC. With the scope set for 1 V/div and 0.5 milliseconds/div, they should appear similar to Figure 3.1-5. Check all four control voltages:

Signal	Location
VCA	U13, pin 8
VCB	U13, pin 14
VCC	U13, pin 7
VCD	U13, pin 1

Check the audio signal waveforms through the following filter stages against the indicated waveform photographs. (These signals result from the test signal which is injected via the jumper between input connector pins 1 and 8.)

Test Point	Waveform	Vert. Scale	Horiz. Scale
U27, pin 7	Figure 3.1-6	1 V/div	0.5 ms/div
U20, pin 8	Figure 3.1-7	1 V/div	0.5 ms/div
U20, pin 14	Figure 3.1-8	1 V/div	0.5 ms/div
U20, pin 1	Figure 3.1-9	1 V/div	0.5 ms/div
U20, pin 7	Figure 3.1-10	2 V/div	0.5 ms/div

Observe the waveform at U16, pin 5, as the bearing calibration control (RC) is varied. With the scope set for 2 V/div and 0.5 milliseconds/div, the waveform should be similar to that shown in Figure 3.1-11. The period during which the waveform is low depends on RC.

Check that the /SQ voltage at U16, pin 9 is a logic high (8 to 9 VDC). Also verify that U9, pin 13 is a logic low (0 to 1 VDC).

Verify the operation of the bearing display logic by checking the following waveforms against the indicated photographs.

Test Point	Waveform	Vert. Scale	Horiz. Scale
U15, pin 10	Figure 3.1-12	2 V/div	0.1 s/div
U9, pin 1	Figure 3.1-13	2 V/div	1 ms/div
U24, pin 1	Figure 3.1-14	2 V/div	1 ms/div
U24, pin 13	Figure 3.1-15	2 V/div	50 µs/div
U25, pin 1	Figure 3.1-16	2 V/div	0.1 ms/div
U25, pin 13	Figure 3.1-17	2 V/div	0.5 ms/div
U17, pin 10	Figure 3.1-18	2 V/div	0.5 ms/div
U17, pin 4	Figure 3.1-19	2 V/div	0.5 ms/div

Observe the signal at U16, pin 13, with the scope set at 2 V/div and 0.2 milliseconds/div. The high period of this waveform will vary as the brightness control (RA) is changed. The waveform should be similar to Figure 3.1-20.

Check that the voltage at U11, pin 3, is a logic low (0 to 1 VDC).

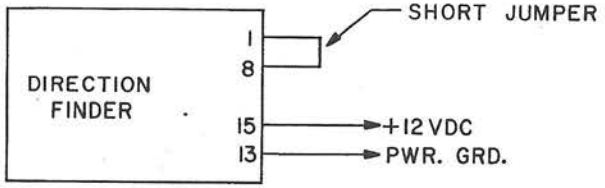


Figure 3.1-1
Self Test Setup

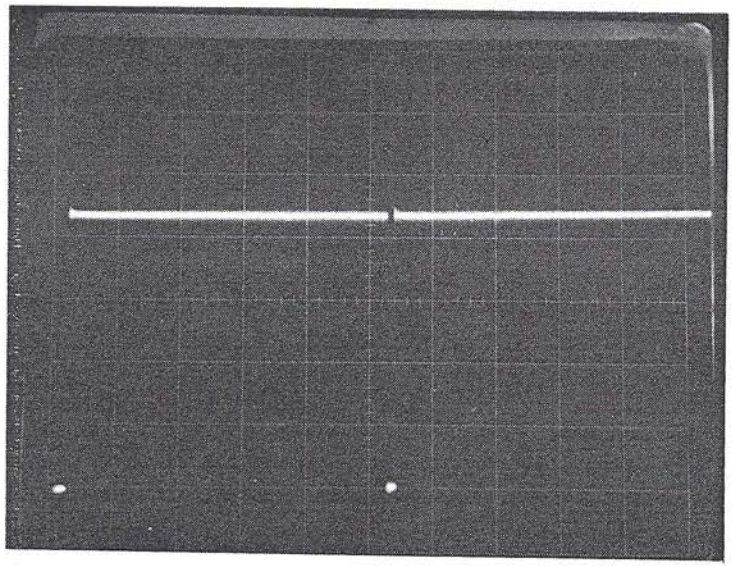


Figure 3.1-3
U12-15 Waveform

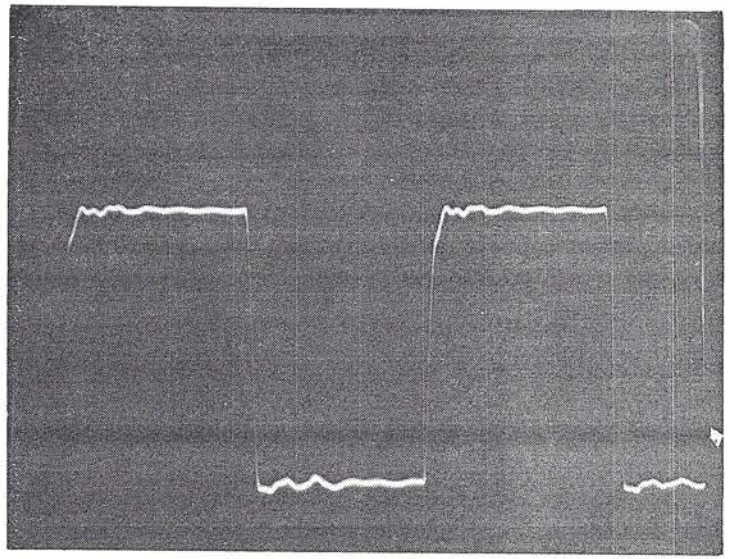


Figure 3.1-2
U6-3 Waveform

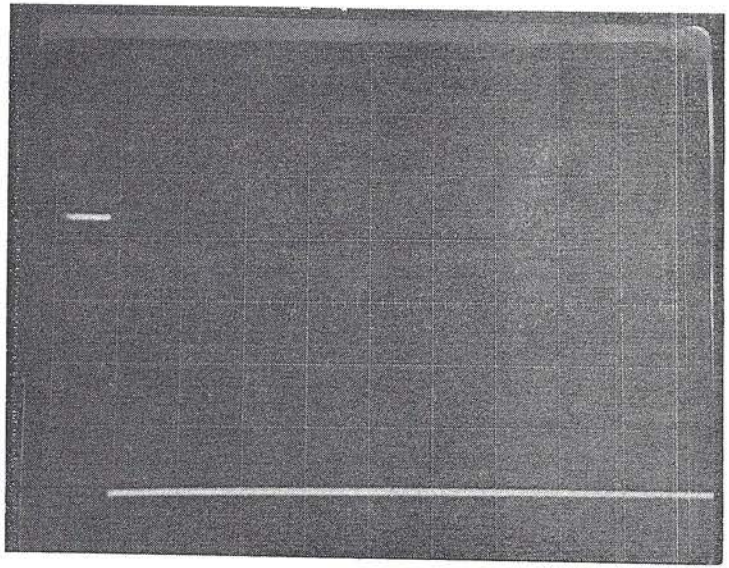


Figure 3.1-4
U16-1 Waveform

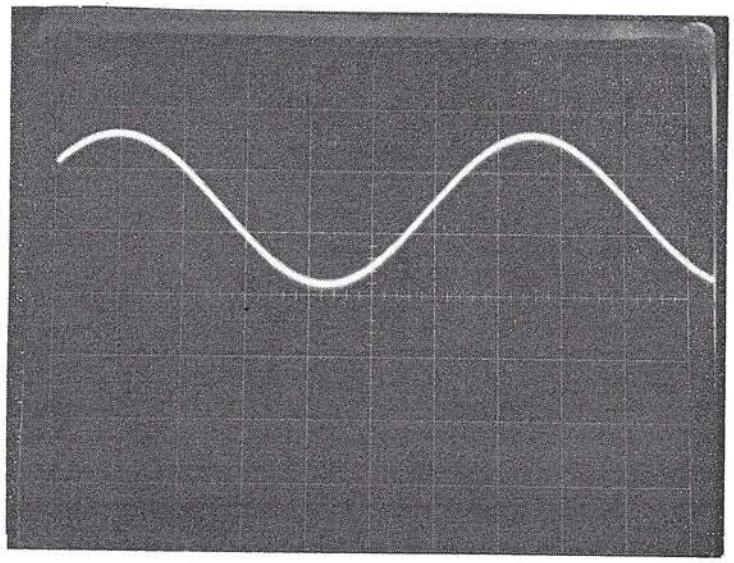


Figure 3.1-5
U13-1,7, 8 and 14 Waveforms

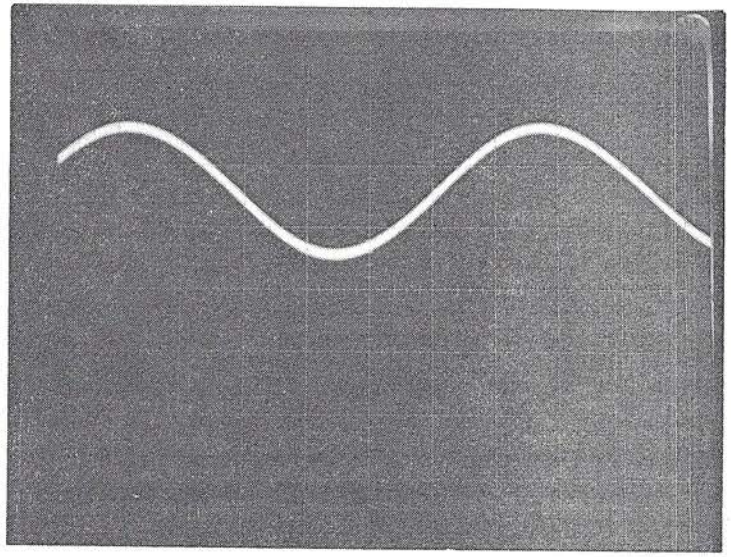


Figure 3.1-6
U27-7 Waveform

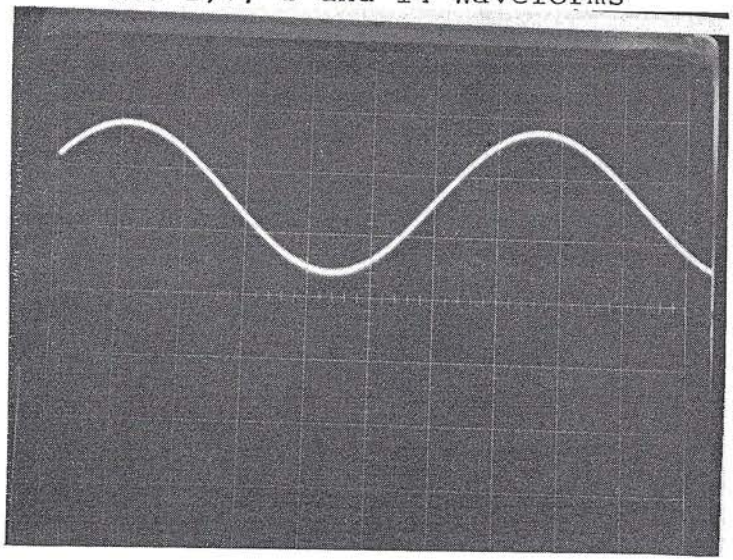


Figure 3.1-7
U20-8 Waveform

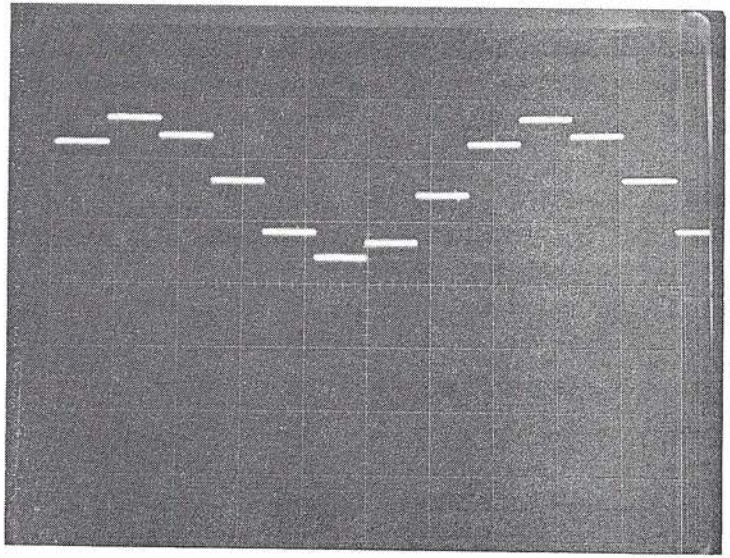


Figure 3.1-8
U20-14 Waveform

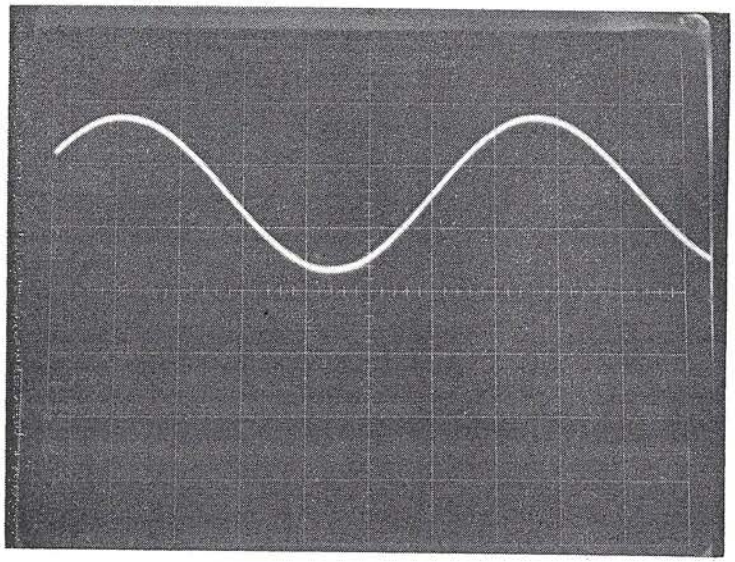


Figure 3.1-9
U20-1 Waveform

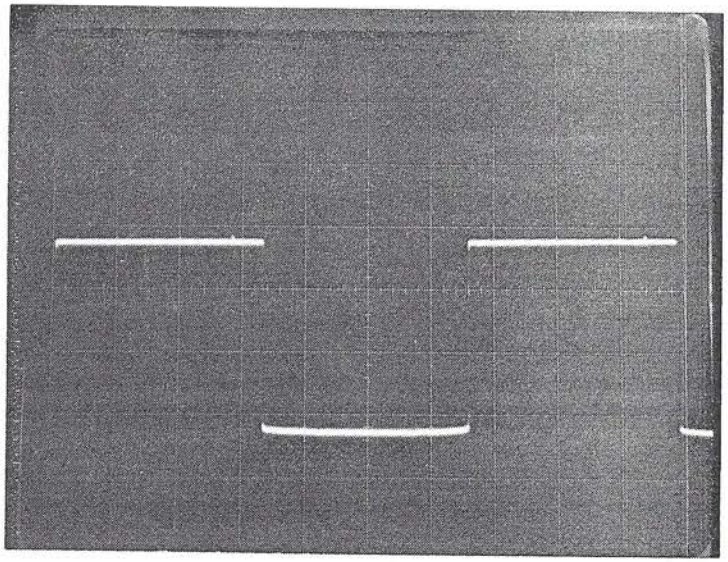


Figure 3.1-10
U20-7 Waveform

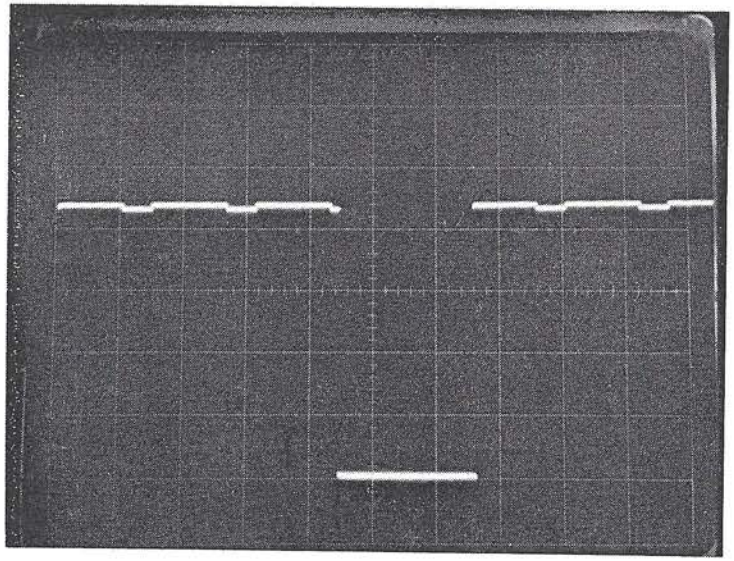


Figure 3.1-11
U16-5 Waveform

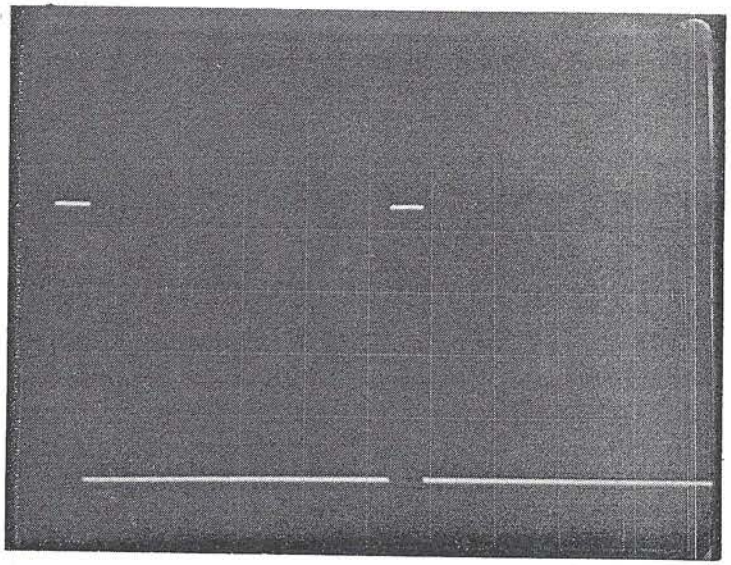


Figure 3.1-12
U15-10 Waveform

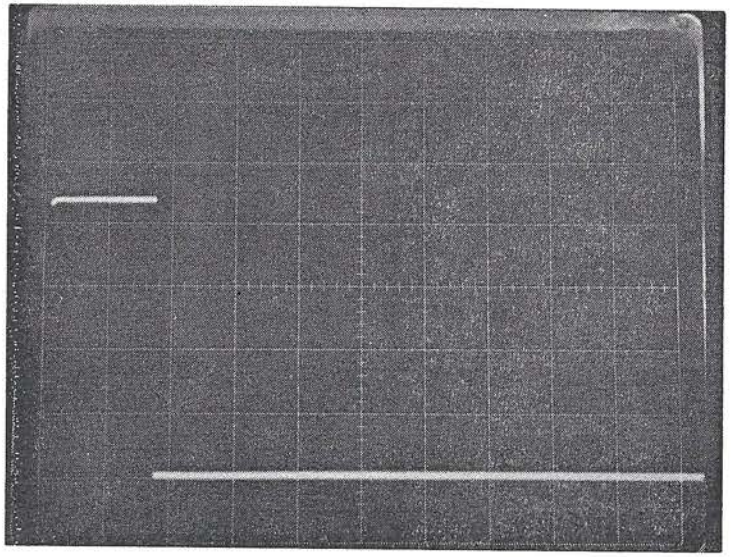


Figure 3.1-13
U9-1 Waveform

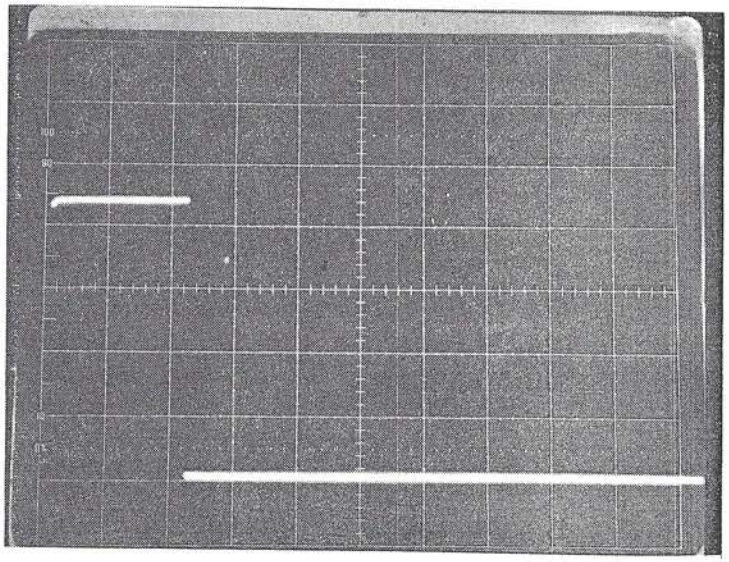


Figure 3.1-14
U24-1 Waveform

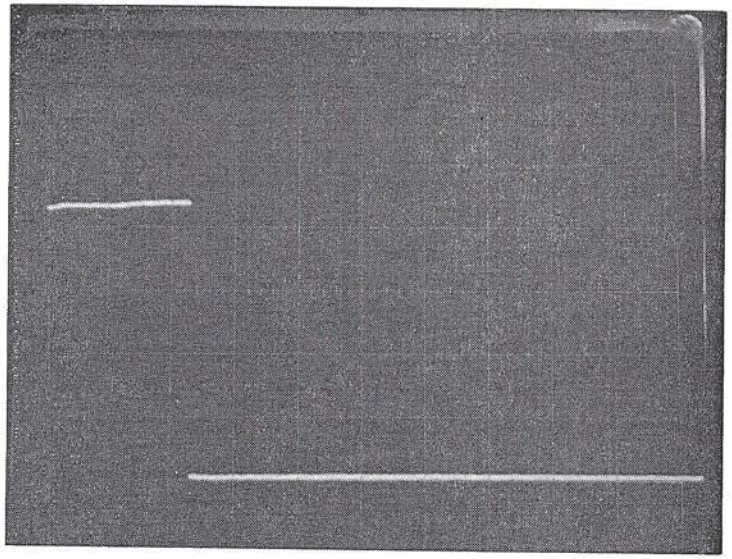


Figure 3.1-15
U24-13 Waveform

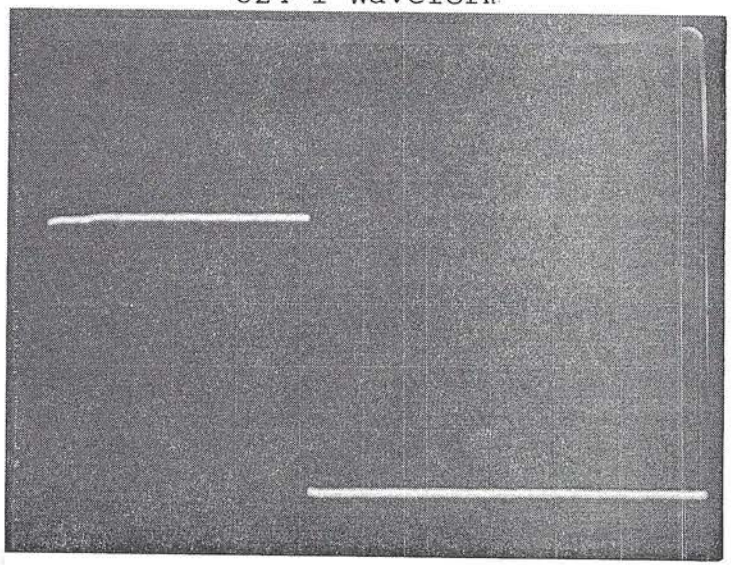


Figure 3.1-16
U25-1 Waveform

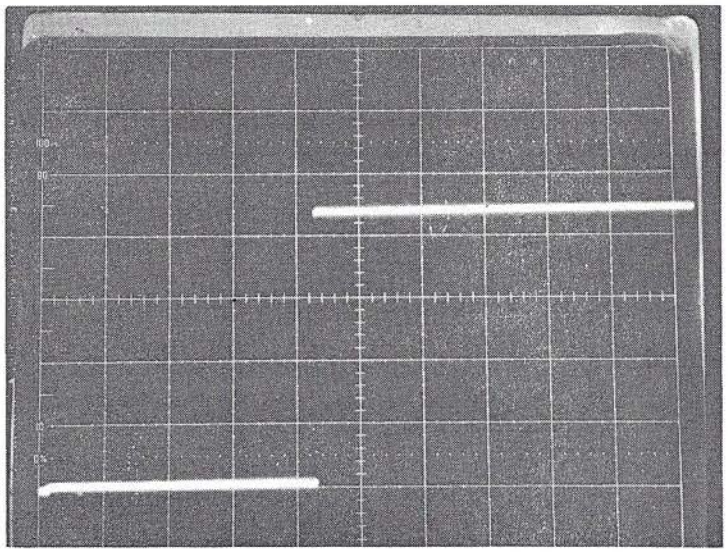


Figure 3.1-17
U25-13 Waveform

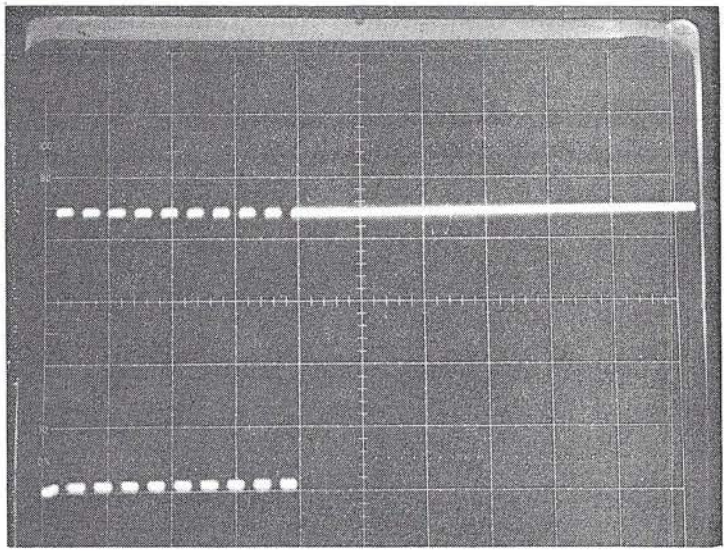


Figure 3.1-18
U17-10 Waveform

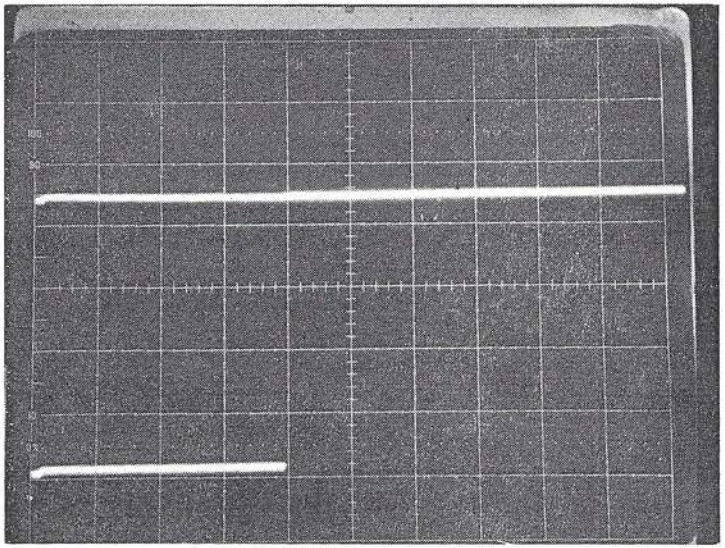


Figure 3.1-19
U17-4 Waveform

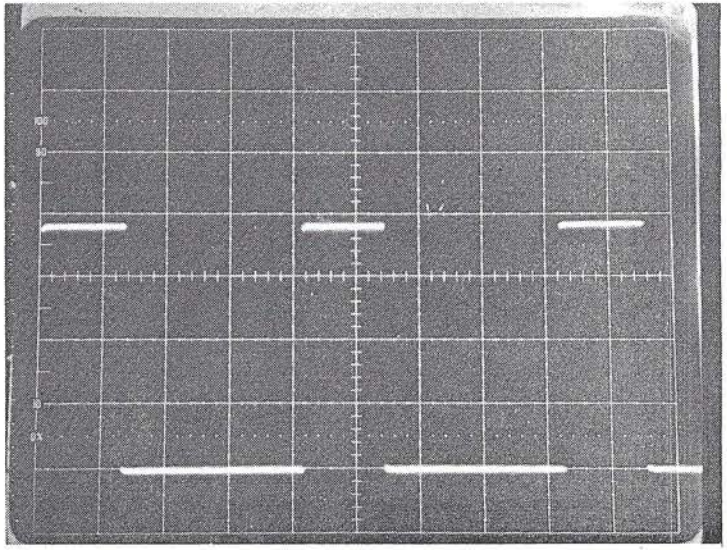


Figure 3.1-20
U16-13 Waveform

3.2 RF SUMMER CHECKOUT

For this measurement, you will need a high bandwidth oscilloscope (at least 20 MHz) and a signal generator. Connect them to the direction finder as shown in Figure 3.2-1.

Set the signal generator for about 25 mVRMS (-19 dBm) at a frequency of approximately 30 MHz. With the scope set at 50 mV/div, 0.5 milliseconds/div, the waveform should be similar to Figure 3.2-2. Move the signal generator output from input A to input B, C, and D. In each case, the waveform should be similar to Figure 3.2-2.

If you have a Model DDF4001 or DDF4002, this completes the detailed checkout. Remove the jumper between pins 1 and 8 on the 15 pin cable connector and reconnect for normal operation as described in Section 2.0.

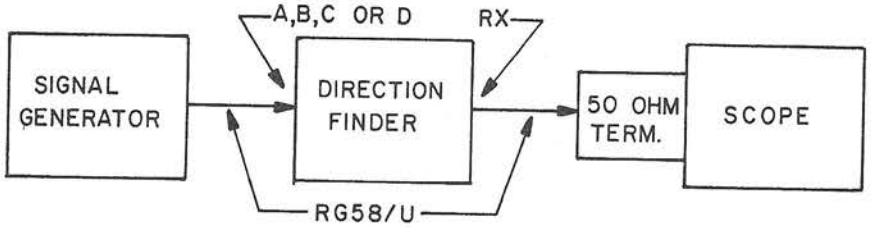


Figure 3.2-1
Setup for RF Summer Checkout

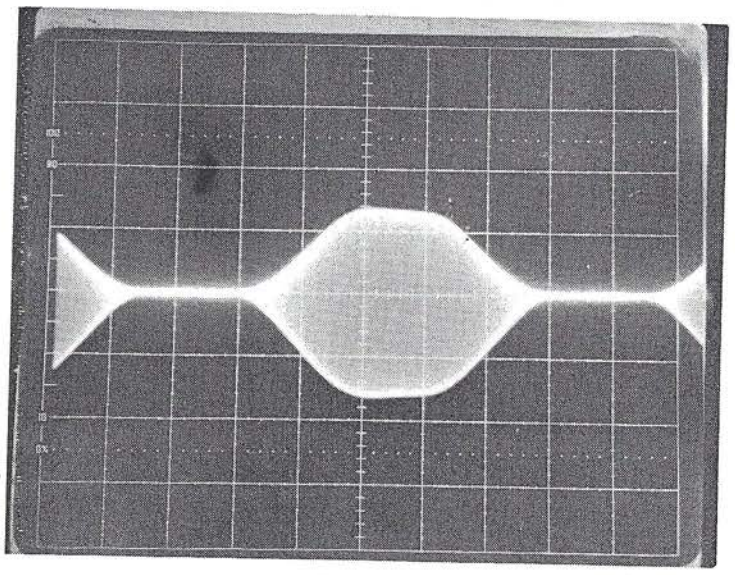


Figure 3.2-2
RF Summer Output Waveform

3.3 SERIAL INTERFACE CHECKOUT (Model DDF4003)

Measure the following power supply voltages on the Serial Interface board (DDF4104).

Test Point	Voltage
U1, pin 14	+9, +/- 0.5 VDC
U1, pin 1	-8, +/- 1.0 VDC
U2, pin 1	+5, +/- 0.25 VDC

Check the following signals against the figures listed.

Test Point	Waveform	Vert. Scale	Horiz. Scale
U9, pin 9	Figure 3.3-1	2 V/div	0.2 milliseconds/div
U5, pin 13	Figure 3.3-2	2 V/div	1 milliseconds/div
U5, pin 1	Figure 3.3-3	2 V/div	1 milliseconds/div
U3, pin 1	Figure 3.3-4	2 V/div	50 milliseconds/div
U7, pin 9	Figure 3.3-5	2 V/div	0.5 milliseconds/div
U8, pin 3	Figure 3.3-6	2 V/div	50 milliseconds/div
U10, pin 1	Figure 3.3-7	2 V/div	1 microseconds/div
U2, pin 25	Figure 3.3-8	2 V/div	50 milliseconds/div

This completes the detailed checkout procedure for Model DDF4003. Remove the jumper between pins 1 and 8 on the 15 pin cable connector and reconnect for normal operation as described in Section 2.0.

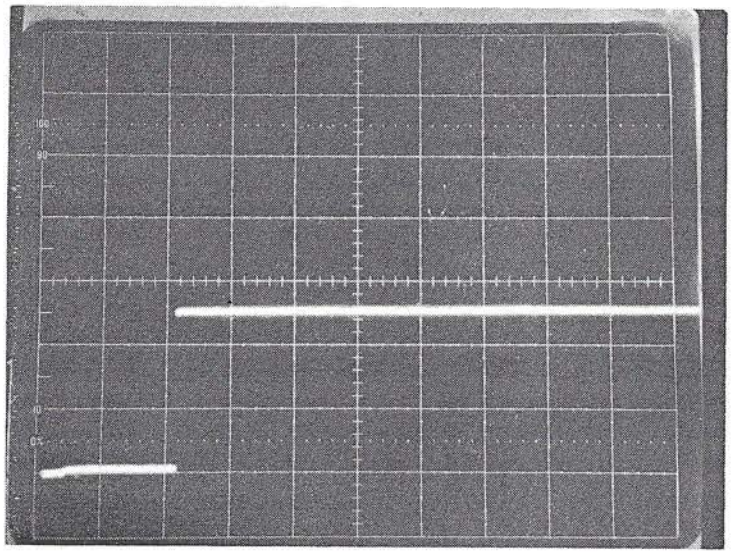


Figure 3.3-1
U9-9 Waveform

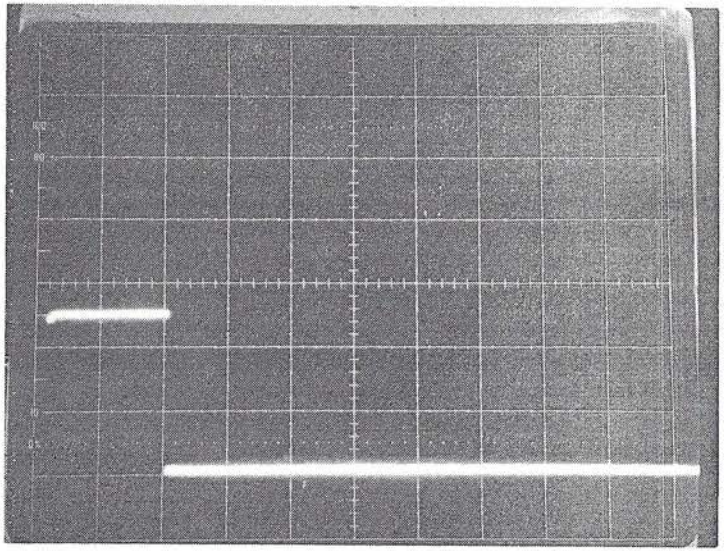


Figure 3.3-2
U5-13 Waveform

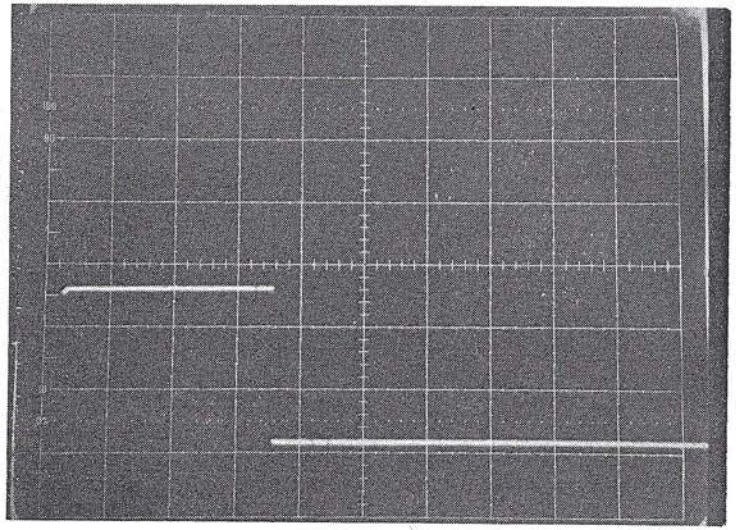


Figure 3.3-3
U5-1 Waveform

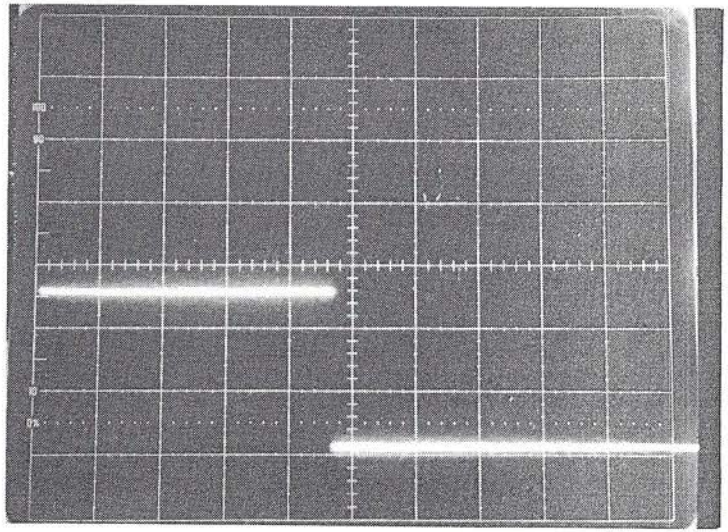


Figure 3.3-4
U3-1 Waveform

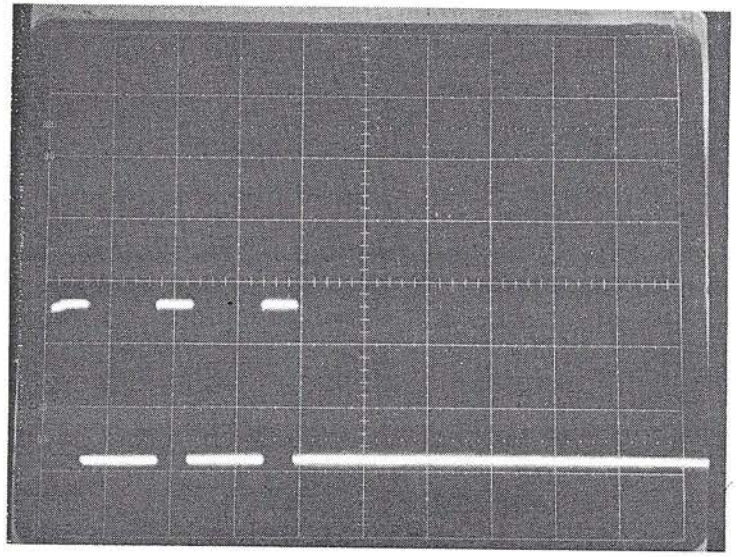


Figure 3.3-5
U7-9 Waveform

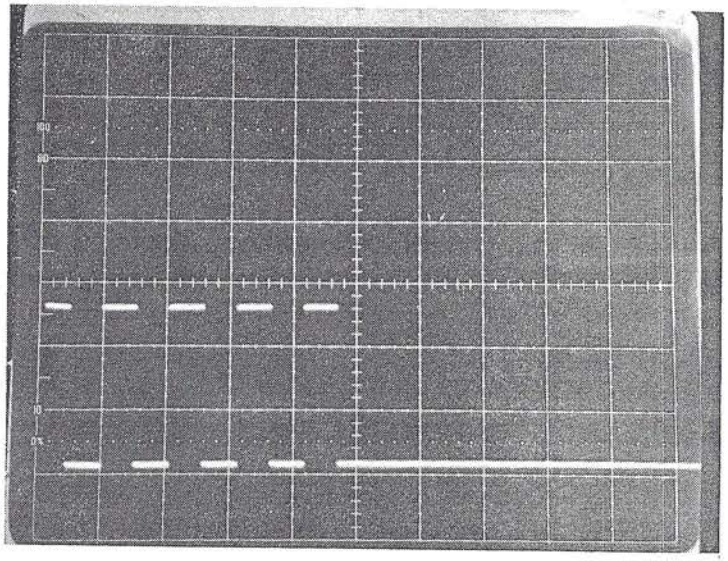


Figure 3.3-6
U8-3 Waveform

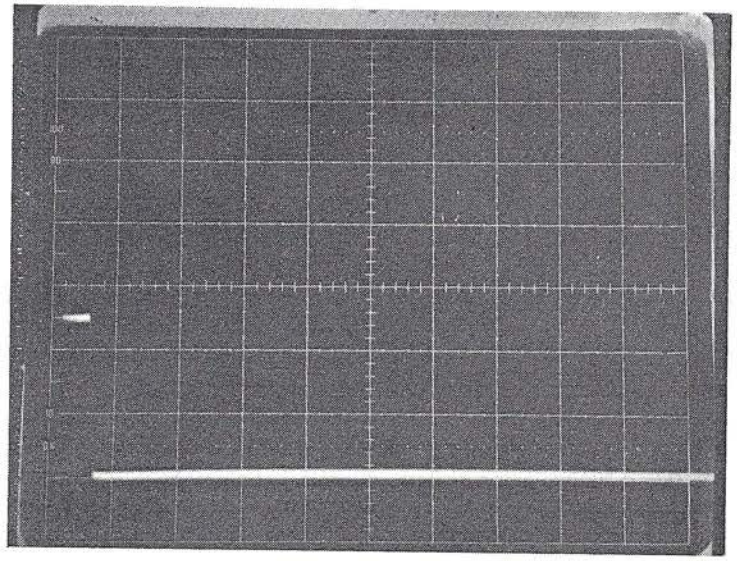


Figure 3.3-7
U10-1 Waveform

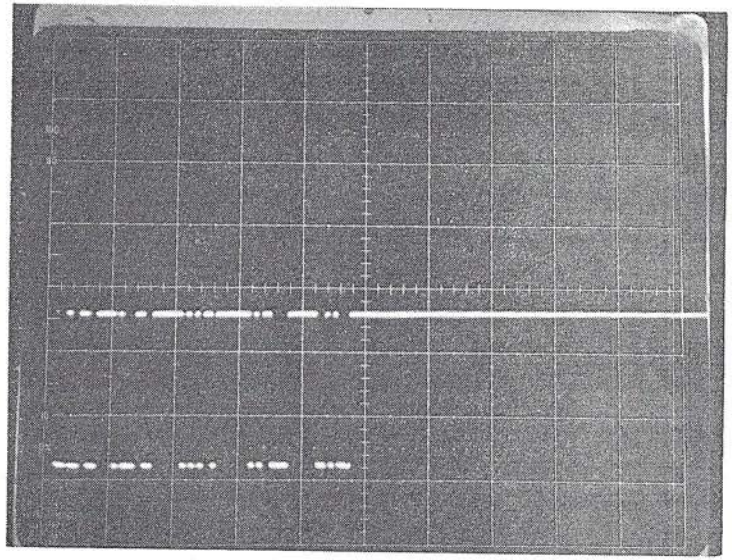


Figure 3.3-8
U2-25 Waveform

3.4 SPEECH SYNTHESIZER CHECKOUT (Model DDF4004)

Measure the following power supply voltages on the Speech Synthesizer board (DDF4105).

Test Point	Voltage
U1, pin 24	+5, +/- 0.25 VDC
U2, pin 40	+9, +/- 0.5 VDC

Check the following signals against the figures listed.

Test Point	Waveform	Vert. Scale	Horiz. Scale
U9, pin 9	Figure 3.4-1	2 V/div	0.2 milliseconds/div
U5, pin 13	Figure 3.4-2	2 V/div	1 milliseconds/div
U5, pin 1	Figure 3.4-3	2 V/div	1 milliseconds/div
U3, pin 1	Figure 3.4-4	2 V/div	0.2 seconds/div
U7, pin 9	Figure 3.4-5	2 V/div	0.5 milliseconds/div
U6, pin 5	Figure 3.4-6	2 V/div	0.2 seconds/div
U8, pin 7	Figure 3.4-7	1 V/div	20 milliseconds/div
U8, pin 1	Figure 3.4-8	2 V/div	20 milliseconds/div

Note that the waveforms observed on U8 above will depend on the word being synthesized.

This completes the detailed checkout procedure for Model DDF4004. Remove the jumper between pins 1 and 8 on the 15 pin cable connector and reconnect for normal operation as described in Section 2.0.

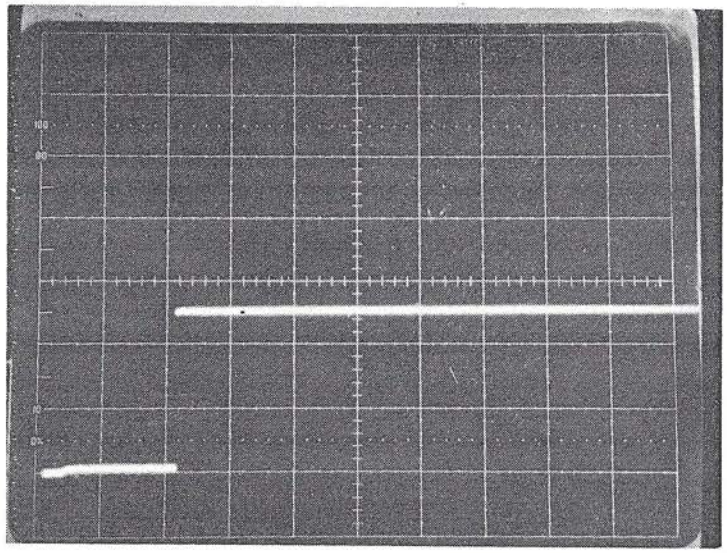


Figure 3.4-1
U9-9 Waveform

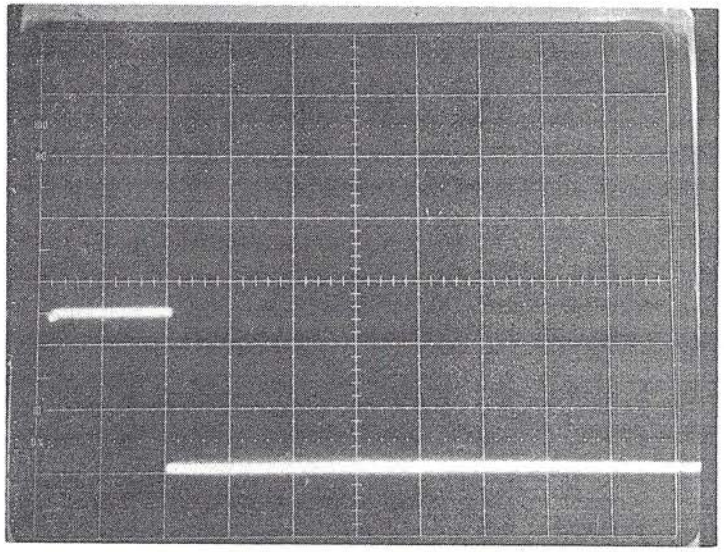


Figure 3.4-2
U5-13 Waveform

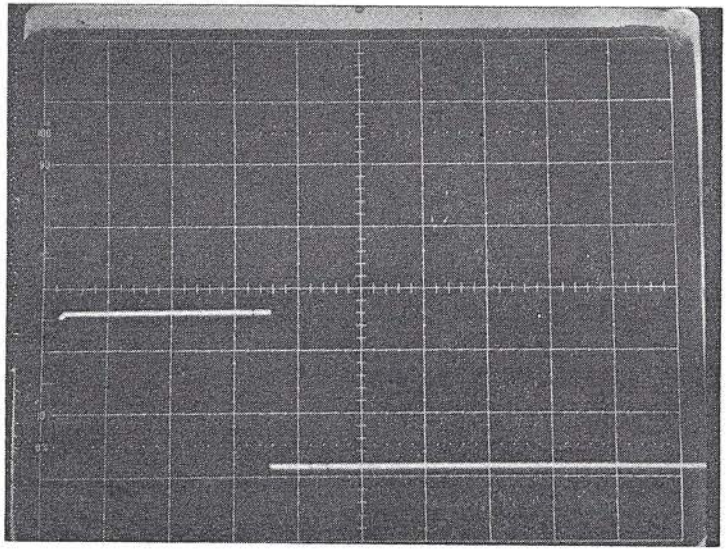


Figure 3.4-3
U5-1 Waveform

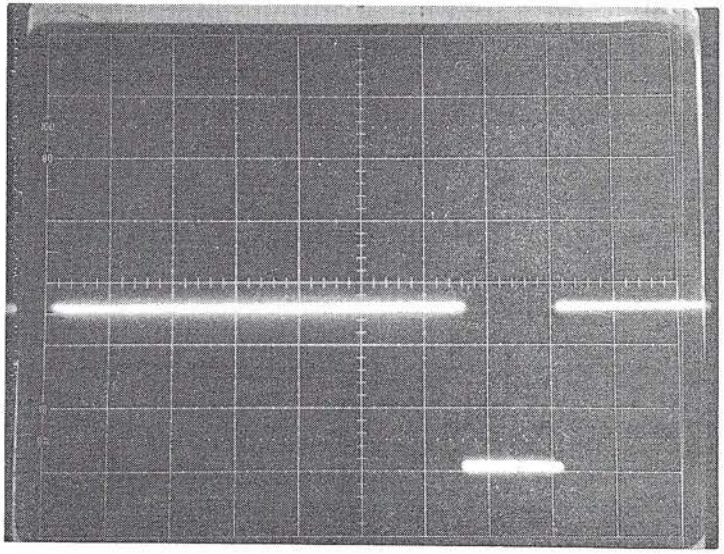


Figure 3.4-4
U3-1 Waveform

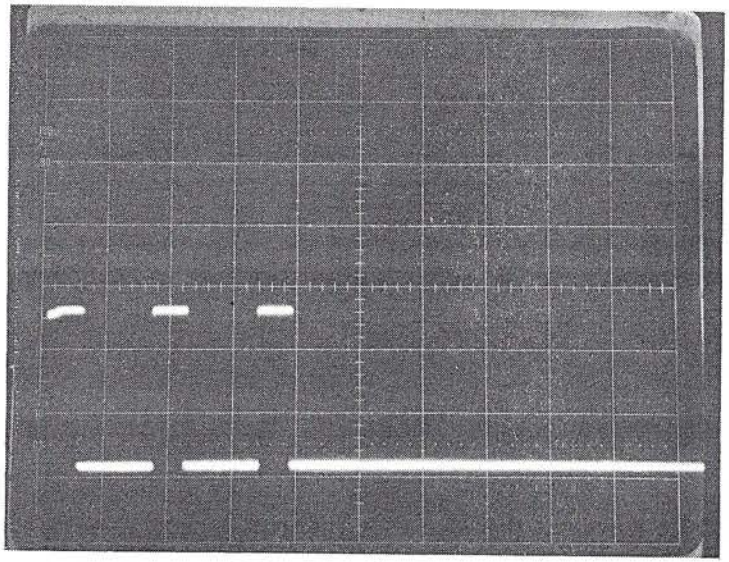


Figure 3.4-5
U7-9 Waveform

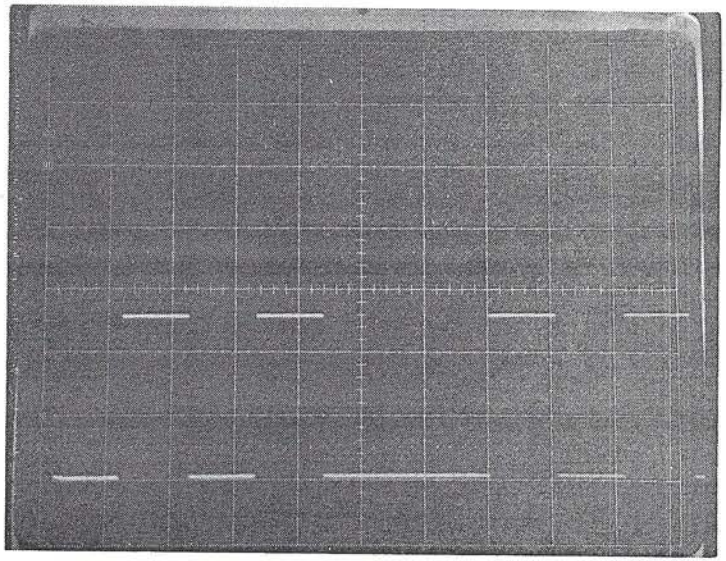


Figure 3.4-6
U6-5 Waveform

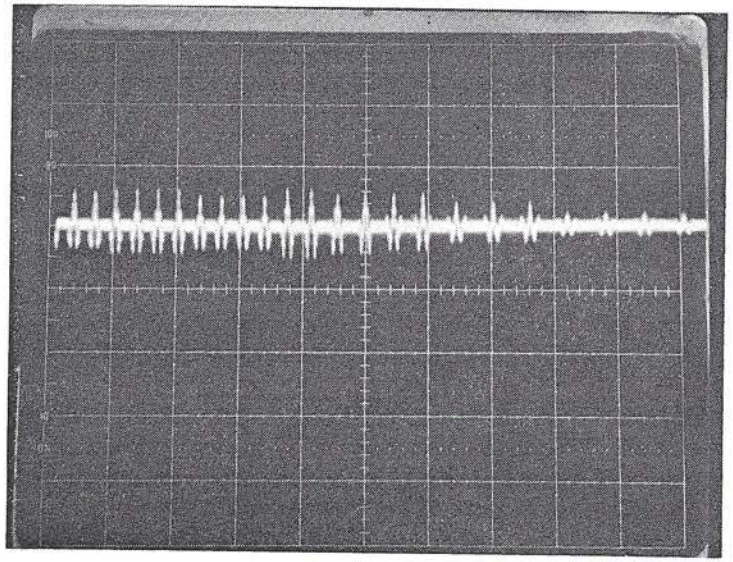


Figure 3.4-7
U8-7 Waveform

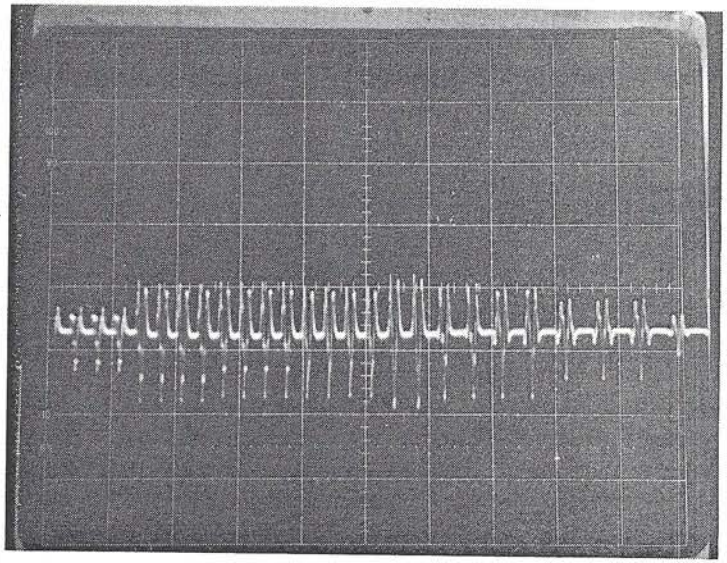


Figure 3.4-8
U8-1 Waveform

Section 4.0
TECHNICAL DESCRIPTION

4.1 THEORY OF OPERATION

Radio direction finding (RDF) systems tend to fall into two general categories depending on whether or not they use the Doppler shift principle. Most non-Doppler RDFs employ directional antennas which produce peaks or nulls in the received signal amplitude as they are rotated. Doppler type systems, on the other hand, detect the frequency modulation imparted to the received signal by translational motion of a nondirectional antenna. As a consequence of the "capture effect" of the FM receiver which detects this frequency modulation, Doppler type systems generally are less sensitive to interfering signals than amplitude measurement systems. The first known RDF based on detecting the Doppler shift was patented by H. T. Budenbom in 1947 and used a motor driven antenna. Doppler RDFs today do not mechanically rotate an antenna, but instead rely on sequential switching between a series of antennas placed in a circular array to approximate a single continuously rotating element.

Sequentially switched arrays, although widely used, are not without problems of their own, however. They are generally large and unwieldy for mobile use at VHF frequencies, and the transients associated with rapidly switching the RF signal between elements frequently result in receiver desensitization and susceptibility to off channel intermodulation. These problems are avoided in your RDF by linearly mixing the RF signals from four antenna elements in a continuous manner. The resultant signal closely approximates that which would be sensed by a single antenna smoothly rotating in a circular path.

The principle behind Doppler direction finding can be explained by considering the geometry shown in Figure 4.1-1 which illustrates a simple antenna located at a distance R_1/λ and an angle θ from the reference position. Assume the incoming signal is located far (relative to the wavelength, λ) from the receiving antenna at the bearing ϕ shown. Then the voltage induced in the antenna can be written as:

$$E_R = A \sin(\omega_c t + \Psi)$$

where A is the received amplitude in volts, ω_c is the carrier frequency in radians per second, t is the time in seconds and is selected to start with a zero crossing of E_R at the origin and Ψ is the phase shift in radians due to the antenna's being closer to or further from the transmitter. If the antenna is closer to the source, Ψ would be positive, indicating a phase lead, etc.

For the geometry shown,

$$\Psi = 2\pi R_1/\lambda \cos(\phi - \theta)$$

Now suppose the receiving antenna is permitted to rotate with velocity ω_d in a circular path of radius R_1/λ. Then $\theta = \omega_d t$ and the phase of the received signal is:

$$\psi(t) = 2\pi R_1/\lambda \cos(\phi - \omega_d t)$$

This equation indicates that the rotating antenna has caused the incoming carrier to become phase (and frequency) modulated. A standard FM receiver will produce an audio output equal to the frequency deviation of the received signal.

$$E_{AUDIO} = K_A 2\pi\omega_d R_1/\lambda \cos(\phi - \omega_d t)$$

Thus the receiver's audio output is a sinusoid, having a frequency equal to the antenna commutation frequency ω_d, and a phase angle equal to the bearing angle ϕ. Electronic processing of the receiver's audio is used to separate the commutation frequency from other frequencies and to measure and display its phase.

Another way of looking at the system is to consider the situation when the rotating antenna is at the angle where it is directly approaching the incoming signal. The maximum relative velocity causes an apparent increase in the carrier frequency at this point. Similarly, when the antenna has moved 180 degrees to the point where it is traveling away from the transmitter, the relative velocity is a minimum, and the carrier frequency appears to be lower. This is the familiar Doppler shift phenomenon, but here the rotation of the antenna produces a periodic up/down shift, the phase of which is set by the bearing angle between receiver and transmitter.

The method used to simulate a physically rotating antenna in your RDF can be explained by referring to Figure 4.1-2. The real antennas are designated A, B, C and D and are located at the corners of a square. Antenna S is simulated by combining the outputs of antennas A through D. Note that S is located on the inscribed circle of radius R_1/λ at the angle θ shown in Figure 4.1-2.

If an incoming signal were arriving from the left or right, the phase at A and B would be equal and the phase at C and D would also be equal. As long as the array is less than 1/2 wavelength on a side, the phase at point S may be computed by interpolating linearly between the phases to the left and right as indicated in the plot directly below the sketch on the antenna array:

$$\text{Phase at S} = \psi_S = \psi_{C \text{ or } D}$$

$$+ (1 + \sin\theta)/2 (\psi_{A \text{ or } B} - \psi_{C \text{ or } D})$$

$$= K_X \psi_{A \text{ or } B} + (1 - K_X) \psi_{C \text{ or } D}$$

$$\text{where } K_X = (1 + \sin\theta)/2$$

For example, if S is midway between A and D, $\theta = 0°$, $K_X = 1/2$, $(1-K_X) = 1/2$ and the phase is the simple average of the phases measured at A and D. If we now consider a signal originating from the top in Figure 4.1-2, the phase at S can be computed from that at A or D and that at B or C by interpolating along the Y direction. Referring to the graph to the left of the antenna:

$$\text{Phase at S} = \psi_S = \psi_{B \text{ or } C} + (1 + \cos\theta)/2\,(\psi_{A \text{ or } D} - \psi_{B \text{ or } C})$$

$$= K_Y\psi_{A \text{ or } D} + (1-K_Y)\psi_{B \text{ or } C}$$

$$\text{where } K_Y = (1 + \cos\theta)/2$$

These equations may be combined to give a two dimensional interpolation of phase.

$$\psi_S = K_XK_Y\psi_A + K_X(1-K_Y)\psi_B + (1-K_X)(1-K_Y)\psi_C + (1-K_X)K_{Y\psi D}$$

The required gain to be applied to ψ_A is:

$$K_A = K_XK_Y = (1 + \sin\theta)\ (1 + \cos\theta)/4$$

which is plotted in Figure 4.1-3. Note that the gain peaks, as would be expected, at 45 degrees where the simulated antenna S is closest to antenna A. A second small gain increase also occurs 180 degrees from this location. The other gains - K_B, K_C and K_D have shapes identical to K_A but are displaced 90 degrees in phase (K_B lags K_A by 90 degrees, etc.)

Strictly speaking, four identical FM receivers would be required to obtain the four phase angles required for mixing in the above equation. A much simpler implementation, which produces essentially the same result when the antennas are closely spaced, can be obtained by amplitude modulating and summing the four RF voltages from the antennas at the input to a single FM receiver. This is the method used in the Doppler Systems 4000 Series Radio Direction Finders.

A simplified functional block diagram of the complete radio direction finding system is shown in Figure 4.1-4. The RF summer combines the outputs of the four antennas through variable gains which are periodic at the system commutation frequency of 300 Hz. The frequency modulated RF signal is applied to a conventional FM receiver which detects the modulation and provides the audio input to the Doppler signal processor via connection to the external speaker output. Synchronous filtering removes the normal voice content leaving a sine wave having the same frequency as was used to modulate the antenna signals and a phase angle equal to the bearing angle. This sine wave acts as a trigger to latch the outputs of digital counters for display of the bearing in a circular LED array and/or a three digit decimal display. An optional serial interface transmits the bearing data displayed by the unit and an optional speech synthesizer articulates the bearing angle through a self-contained loudspeaker.

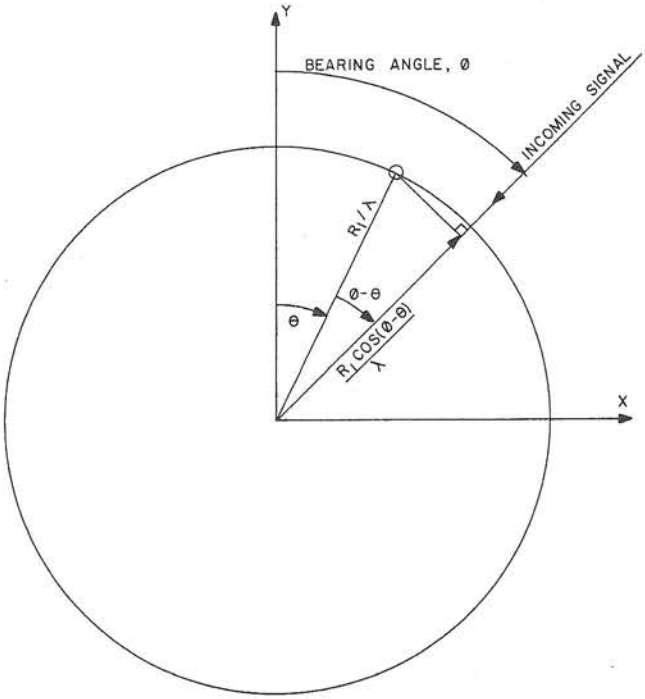


Figure 4.1-1
Doppler Direction Finding Antenna Geometry

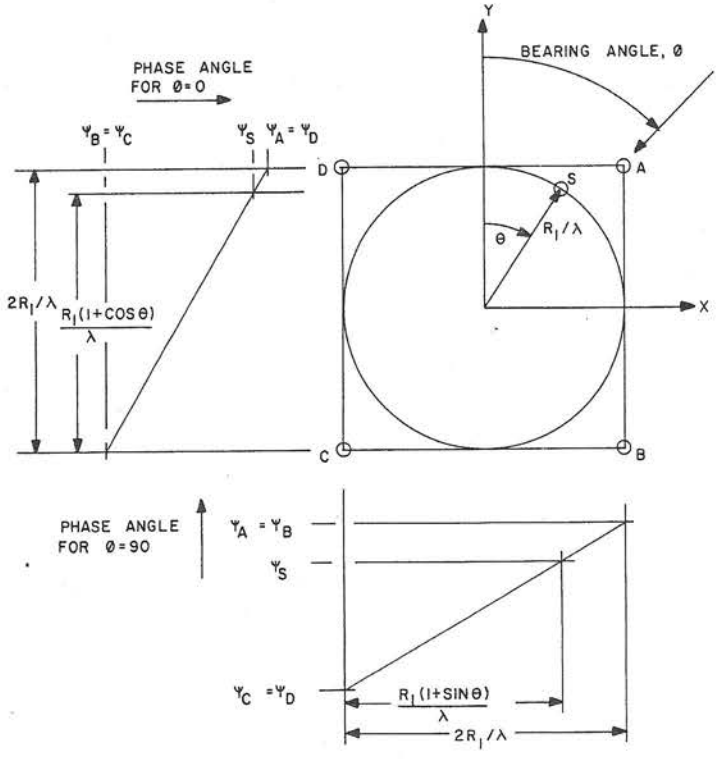


Figure 4.1-2
Phase Angle Interpolation Using Four Antennas

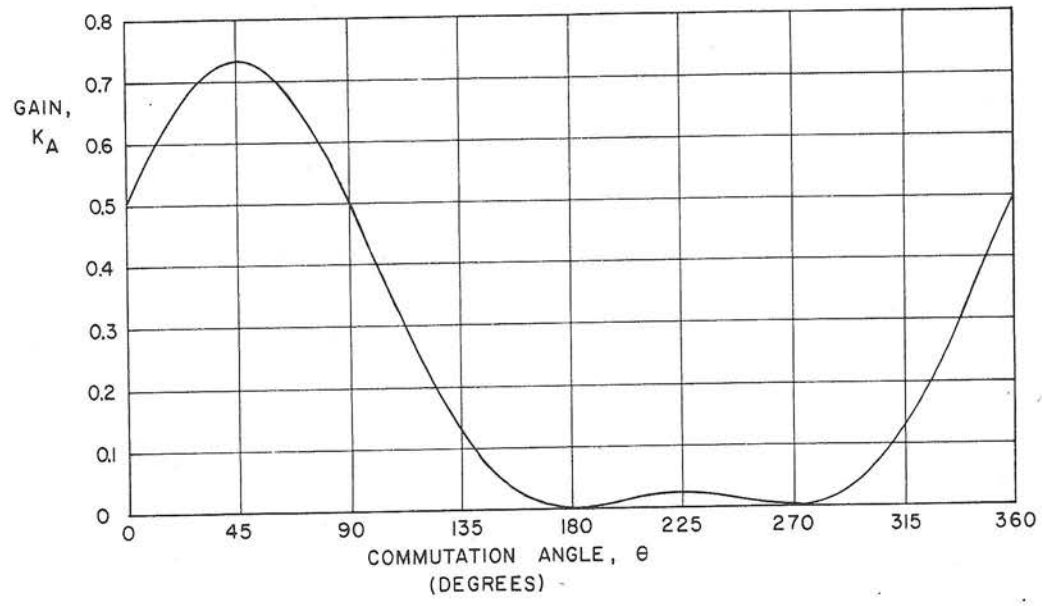


Figure 4.1-3
Phase Angle A Gain Required to Simulate Continuous Rotation

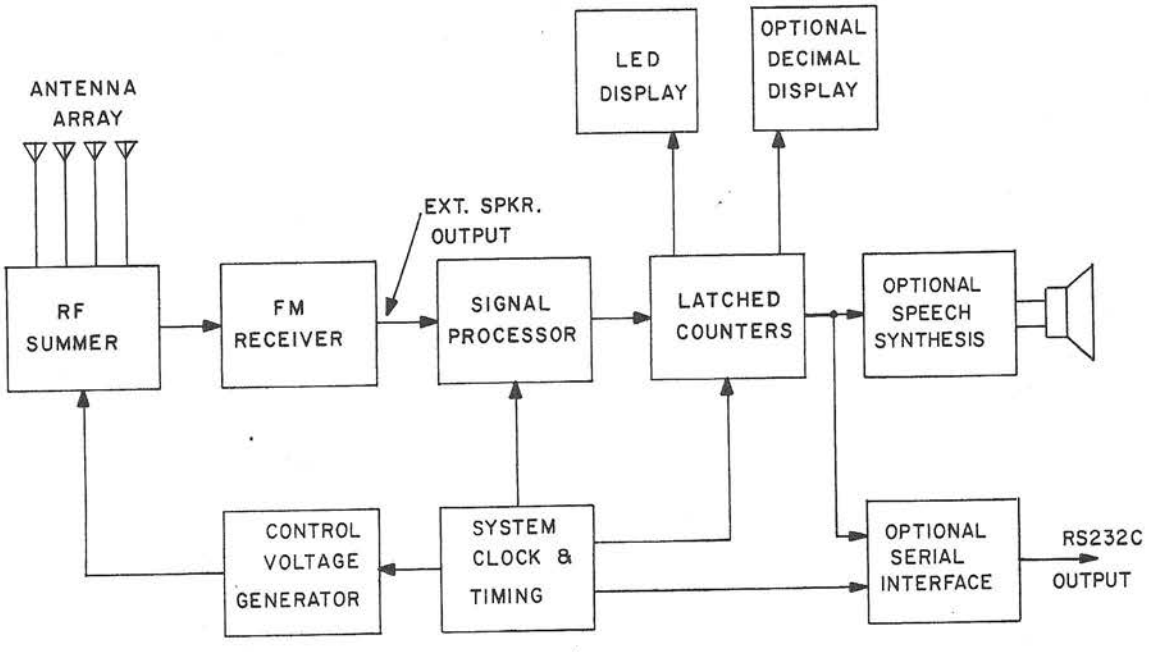


Figure 4.1-4
Block Diagram of Complete Direction Finding System

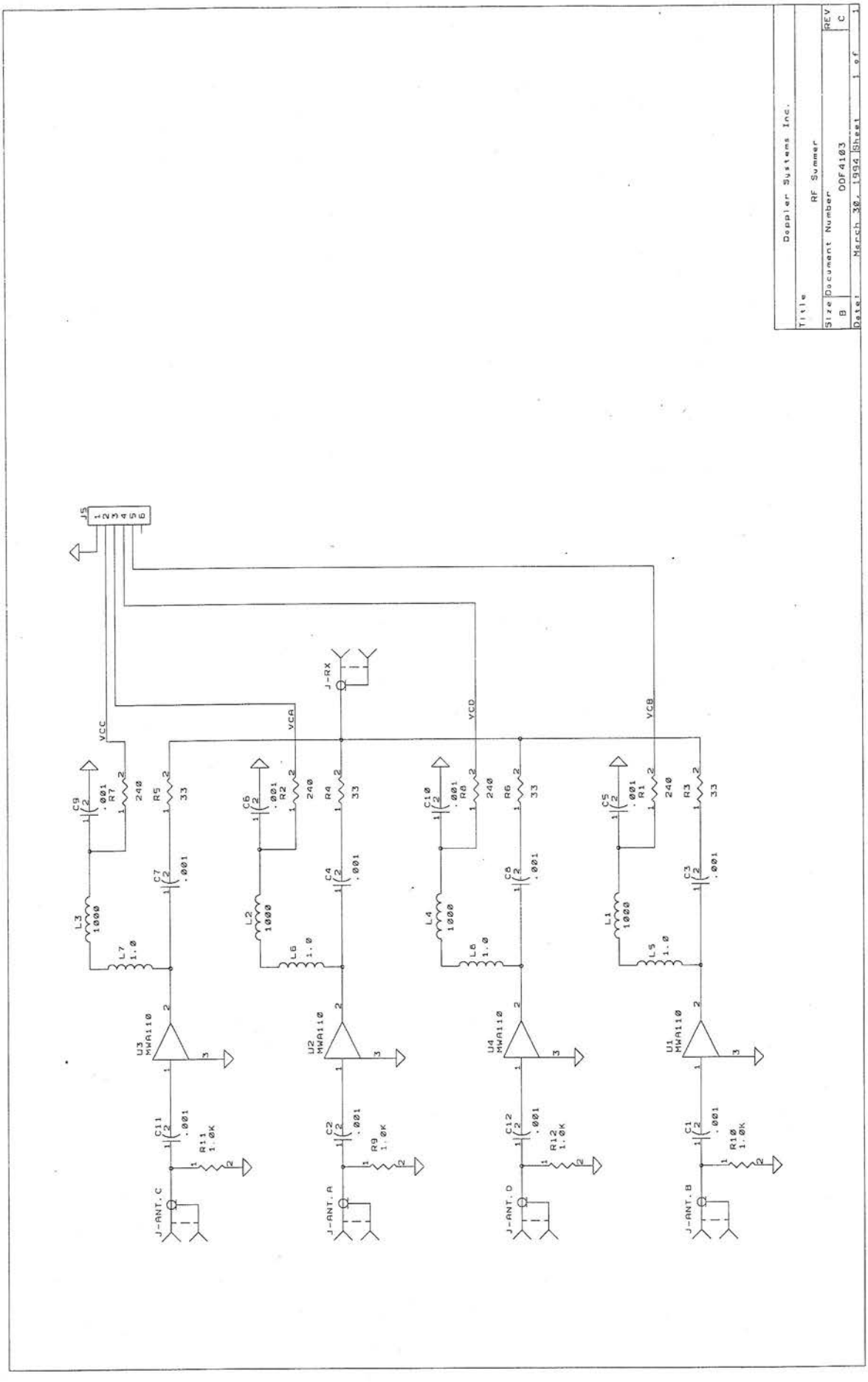
4.2 RF SUMMER

Four voltage controlled preamplifiers are used to amplitude modulate the RF signals developed in each of the four antennas. The outputs from these preamplifiers are then voltage summed and the composite signal sent to the receiver. Although the individual channels are amplitude modulated, the composite signal is phase modulated at the system commutation frequency of 300 Hz. The RF summer circuit provides 50 ohm input and output impedances and avoids the use of tuned circuits which would require matching between channels.

Figure 4.2-1 is the schematic of the RF Summer. MWA-110 hybrid amplifiers are used in each channel. The control voltages are applied to each preamp through 240 ohm resistors which set the correct current range. Control voltages vary from 3.0 to 6.0 VDC. The large RF chokes block any noise on the control voltages to these preamplifiers which could pass through to the receiver front end. The 33 ohm series resistors - together with the preamplifier output impedances of 50 ohms and the receiver input impedance of 50 ohms - form a resistive summer having a 50 ohm output and presenting a 50 ohm load to each preamplifier.

The RF Summer is contained on printed wiring board DDF4103 within a separate shielded subassembly.

Figure 4.2-1


Doppler Systems Inc.
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Date:
March 30, 1994
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VCC
VCA
VCD
VCB
J-RX
C9
.001
R7
240
R5
33
C7
.001
L3
1000
L7
1.0
U3
MWA110
C11
.001
R11
1.0K
J-ANT.C
C6
.001
R2
240
R4
33
C4
.001
L2
1000
L6
1.0
U2
MWA110
C2
.001
R9
1.0K
J-ANT.A
C10
.001
R8
240
R6
33
C8
.001
L4
1000
L8
1.0
U4
MWA110
C12
.001
R12
1.0K
J-ANT.D
C5
.001
R1
240
R3
33
C3
.001
L1
1000
L5
1.0
U1
MWA110
C1
.001
R10
1.0K
J-ANT.B

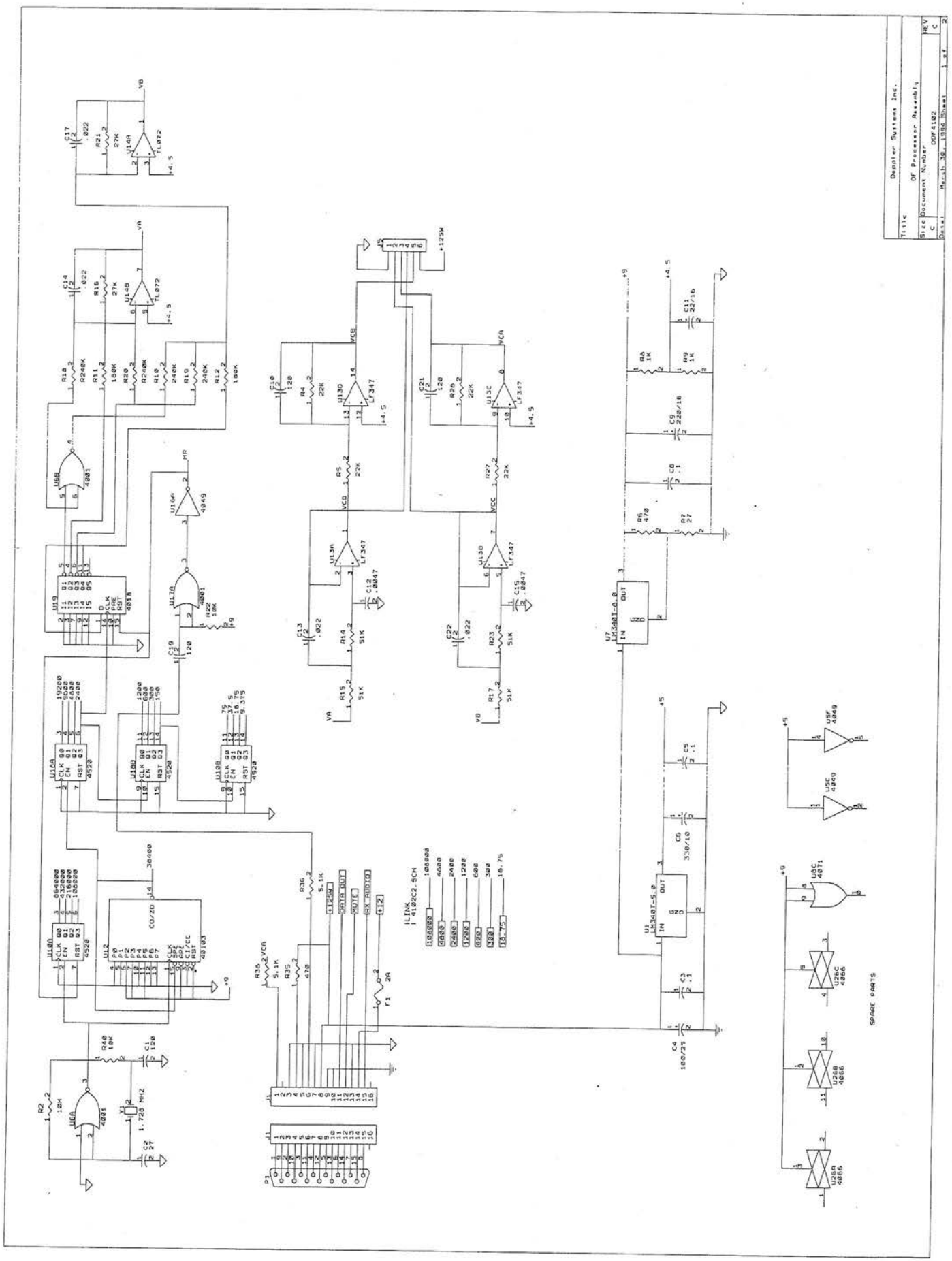
4.3 CONTROL VOLTAGE GENERATION

The Control Voltage Generator provides four-phase 300 Hz offset sinusoids to the Current Driver. It is located on the Processor board, DDF4102, and comprises the circuitry in the right hand area of Figure 4.3-1.

U19 is connected as a divide by 8 walking ring counter driven by a 2400 Hz square wave. The counter is reset each commutation cycle (300 Hz) by a pulse from the master reset, MR. This ensures synchronization with the bearing display counters.

The four counted outputs at pins 5, 4, 6 and 11 are 300 Hz square waves which are staggered by 1 clock count (1/2400 sec.) in time. Outputs 5, 4 and 6 are summed through resistor networks in amplifiers U14A and U14B to synthesize a staircase approximation to a sine and cosine waveform. Feedback filtering in these amplifiers partially smooths these waveforms eliminating the higher frequency components. Amplifiers U13A and U13B provide additional filtering so as to produce nearly pure 300 Hz sinusoids for control voltage phases VCC and VCD. Amplifiers U13C and U13D act as unity gain inverters to generate the remaining two control voltages, phases VCA and VCB.

Figure 4.3-1


Doppler Systems Inc.
Title
DF Processor Assembly
Size Document Number DDF4102 REV C
Date: March 30, 1996 Sheet 1 of 2
SPARE PARTS

4.4 POWER SUPPLY AND CLOCK

This circuitry is located on the Processor Board, DDF4102, and is shown schematically in Figure 4.3-1.

U1 and U7 are linear voltage regulators arranged to provide filtered +5 and +9 VDC to the remainder of the circuitry used on the Processor, Display and RF Summer boards. (Independent voltage regulators are used on the optional Serial Interface and Speech Synthesizer boards.)

Gate U6A is biased for linear operation and contains a crystal feedback circuit to generate a square wave clock signal at 1.728 MHz. Synchronous counter U10A divides this signal by 16 to generate 108000 Hz for use in the 3 digit display logic.

Counter U12 is an 8 stage presettable synchronous down counter connected to divide the system clock frequency by 45. Its output is a short (0.58 microsecond) negative going pulse train at 38400 Hz.

This signal is further divided by a chain of synchronous binary counters - U18A, U18B and U10B to produce square wave clock frequencies of 4800, 2400, 1200, 600, 300 and 18.75 Hz.

To maintain synchronization between the various counters used, a master reset pulse, MR, is generated by gate U17A and invertor U16A. MR consists of a 300 Hz positive going pulse train. Each pulse is approximately 1 microsecond wide.

4.5 AUDIO SIGNAL PROCESSING

The receiver audio output contains a 300 Hz component, the phase of which (relative to the 300 Hz clock signal) is the bearing angle to the transmitter. The audio processing circuitry amplifies and filters this signal from other noise or audio signals recovered by the FM receiver. Figure 4.5-1 contains the schematic of the Audio Signal Processing circuitry.

Amplifier U27A is a compandor device which is connected as an automatic level control. The output, at pin 7, is biased to 4.5 VDC and the ALC gain is such that the AC component of the output will be approximately 2.2 V peak to peak for inputs between 10 MVRMS and 2.0 VRMS.

Frequencies above 300 Hz are attenuated by amplifier U20C which is connected as a unity gain low pass filter.

The 8 section commutative filter comprising analog multiplexer U21, capacitor network U22 and follower amplifier U20D provides a 300 Hz

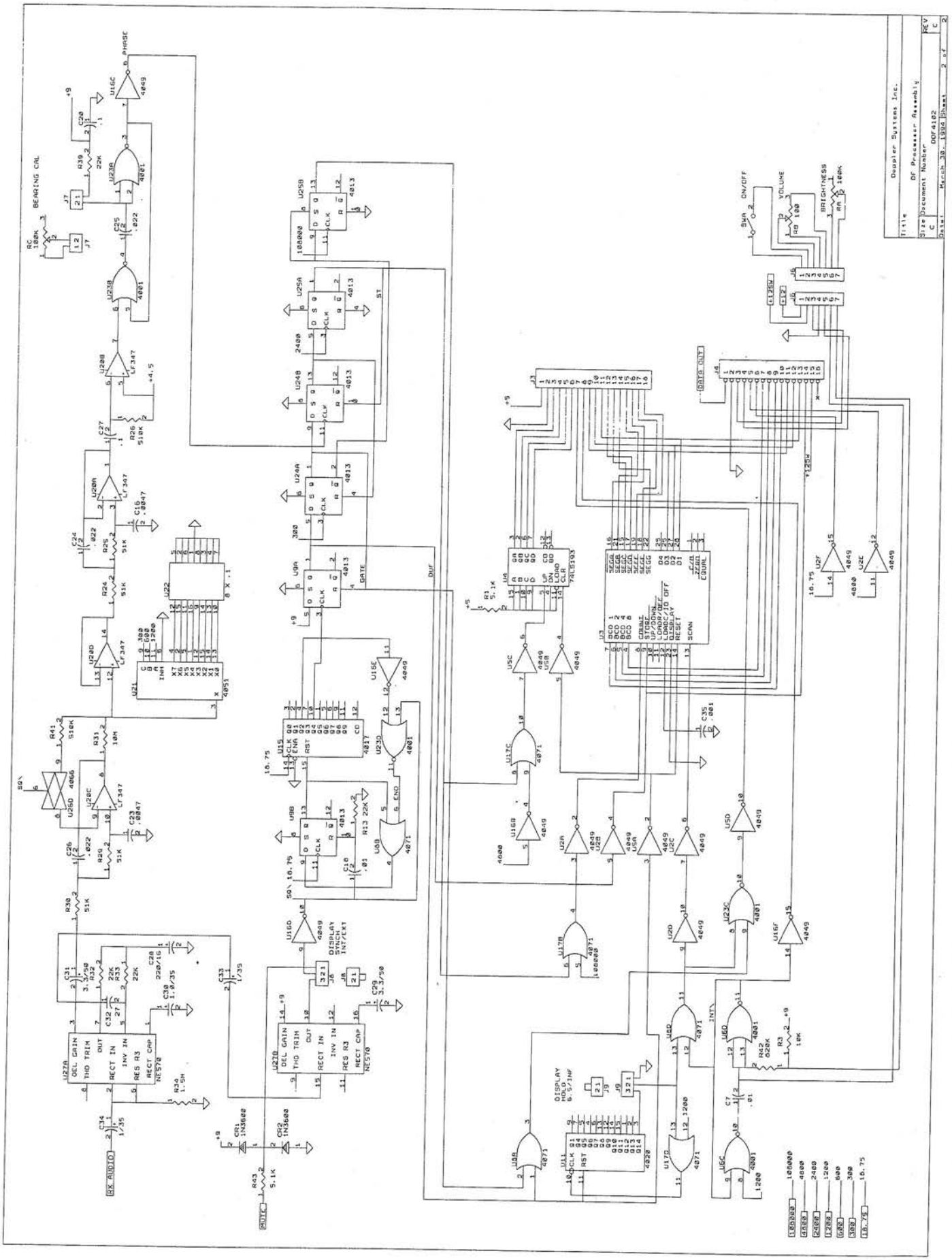
bandpass synchronized to the system 300 Hz clock. The effective Q of this circuit is very high (approximately 400) so that practically all undesired signal components are eliminated. In this filter, the 1/300 second commutation interval is subdivided into 8 equal lengths (1/2400 = 0.417 milliseconds long) during which one of the 8 capacitors in U22 is connected through resistor R31 or R41 to U20C. This RC time constant is long compared to the connection interval, so a number of commutation cycles are required to develop a steady state voltage across the capacitors. This steady state voltage corresponds to the average voltage taken across the same fraction of the 300 Hz clock period. Any frequency which is not synchronous with this clock will therefore average out to zero over a period of many 300 Hz cycles. Amplifier U20D is a unity gain voltage follower which buffers the capacitor voltages through a very high input impedance. The output of U20D is a staircase shaped approximation of the 300 Hz component in the audio input.

When a signal is being received, /SQ is high, and the commutating filter capacitors are connected through resistor R41 by analog switch U26C to amplifier U20C. Resistor R31, which is in parallel with this path, is much larger, so the effective time constant is determined by R41. When no signal is present, the commutating filter discharges more slowly through R31. This arrangement permits bearing phase data to be averaged between pulses if, for example, a series of short (250 millisecond) pulses is being received every second or so.

Amplifier U20A is another unity gain low pass filter which attenuates the higher frequency components in the staircase waveform at U20D.

U20B is used as a comparator on the filtered audio signal which generates a square wave digital logic level signal. Gates U23A and U23B form a variable one-shot which are triggered by a positive going edge on the square wave. The high level interval at the output of U23A is determined by the bearing calibration control setting, RC. This is inverted by U16C so that the low level interval at the output of U16C (PHASE) is adjustable using RC. The rising edge at the end of this interval is used as a trigger in the bearing phase measurement circuit described below.

Figure 4.5-1


Doppler Systems Inc.
DF Processor Assembly
DOF4102
March 30, 1994
BEARING CAL
VOLUME
BRIGHTNESS
ON/OFF
RX AUDIO
MUTE
DISPLAY
SYNCH
INTERFACE

4.6 DISPLAY LOGIC

Compandor U27B is configured to act as an audio level detector. The average audio input at pin 15 controls the gain between pin 14 (+9 VDC) and the output. Since the compandor contains a high gain inverting amplifier, its output will be high (+9 VDC) when no signal is present (receiver squelched). If an external mute signal is available, it may be used in place of the U27B squelch signal. U16D inverts this signal (+9 VDC now corresponds to signal present).

The display control logic updates at a rate of 1.875 Hz and requires that an input be present for at least 150 milliseconds to update. This is accomplished with the start up logic built around D flip flop U9B and decade counter U15. With no signal present U9B will be high (set) which holds U15 reset (all outputs low). When a signal occurs, /SQ becomes high which resets U9B. Counter U15 now begins counting its 18.75 Hz input. A test is performed at the beginning of the third count interval, which could occur between 2 and 3 clock intervals (107 to 160 milliseconds) following the initial /SQ low to high transition. If the /SQ signal is still high (signal present), the display update process continues as explained below. If, however, /SQ is low (no signal), flip flop U9B is set which in turn resets U15 thereby discontinuing the update cycle.

Assuming the signal to be present, counter U15 will output a pulse during the 4th clock interval which commands the following logic to update the display. Because U15 is a divide by 10 counter, succeeding display updates will continue to be commanded at a 1.875 Hz rate (533 milliseconds) as long as the signal is present.

U9A is a D flip flop which is set by the leading edge pulse from counter U15. Flip flop U24A is then set at the next leading edge transition of the 300 Hz clock. When this occurs, U9A is reset. The leading edge on the PHASE signal produced by the Audio Signal Processor circuit described above, sets flip flop U24B whenever U24A is set. When U24B sets, it resets U24A. Hence U24A's output is a single pulse with a leading edge coincident with the 300 Hz clock and a trailing edge determined by the PHASE signal. This signal is labeled GATE on the schematic, and it is used to control the accumulation of counts in the binary and BCD counters.

To reset U24B, an additional flip flop U25A, is used to generate a short reset pulse, ST. The period of this pulse is 1/2400 = 417 microseconds.

4800 Hz clock pulses are gated through U17C during the time interval defined by U24A (GATE). These are translated from +9 to +5 VDC logic levels by invertor U5C and applied to 4-stage binary

counter U4. The four binary outputs from this counter represent this time interval. Since the maximum interval is 1/300 seconds, the maximum count is 4800/300 = 16. This output is decoded and used to drive the 16 LEDs on the Display board.

108000 Hz clock pulses are similarly gated through U17B, translated to +5 DC level and applied to BCD counter U3. The maximum count here would be 108000/300 = 360. The purpose of flip flop U25B is to suppress one pulse from the input to U3 so that the decimal count will be between 0 and 359.

Counters U3 and U4 are reset to zero at the beginning of the display update interval through invertor U5A. The BCD count itself is latched at the end of the gate interval by the .417 millisecond pulse, ST, through U2B. U3 contains a display multiplexer and driver which drives the three common anode seven segment displays directly. It also provides a multiplexed BCD output of each counter stage which is used by the Serial Interface and Speech Synthesizer circuits.

Display brightness is controlled by RA which sets the off interval of the 1200 Hz pulse train generated by one-shot U6C/U6D. This pulse train (/INT) is buffered by invertor U16F to drive the center Power On LED via a buffer transistor on the Display board.

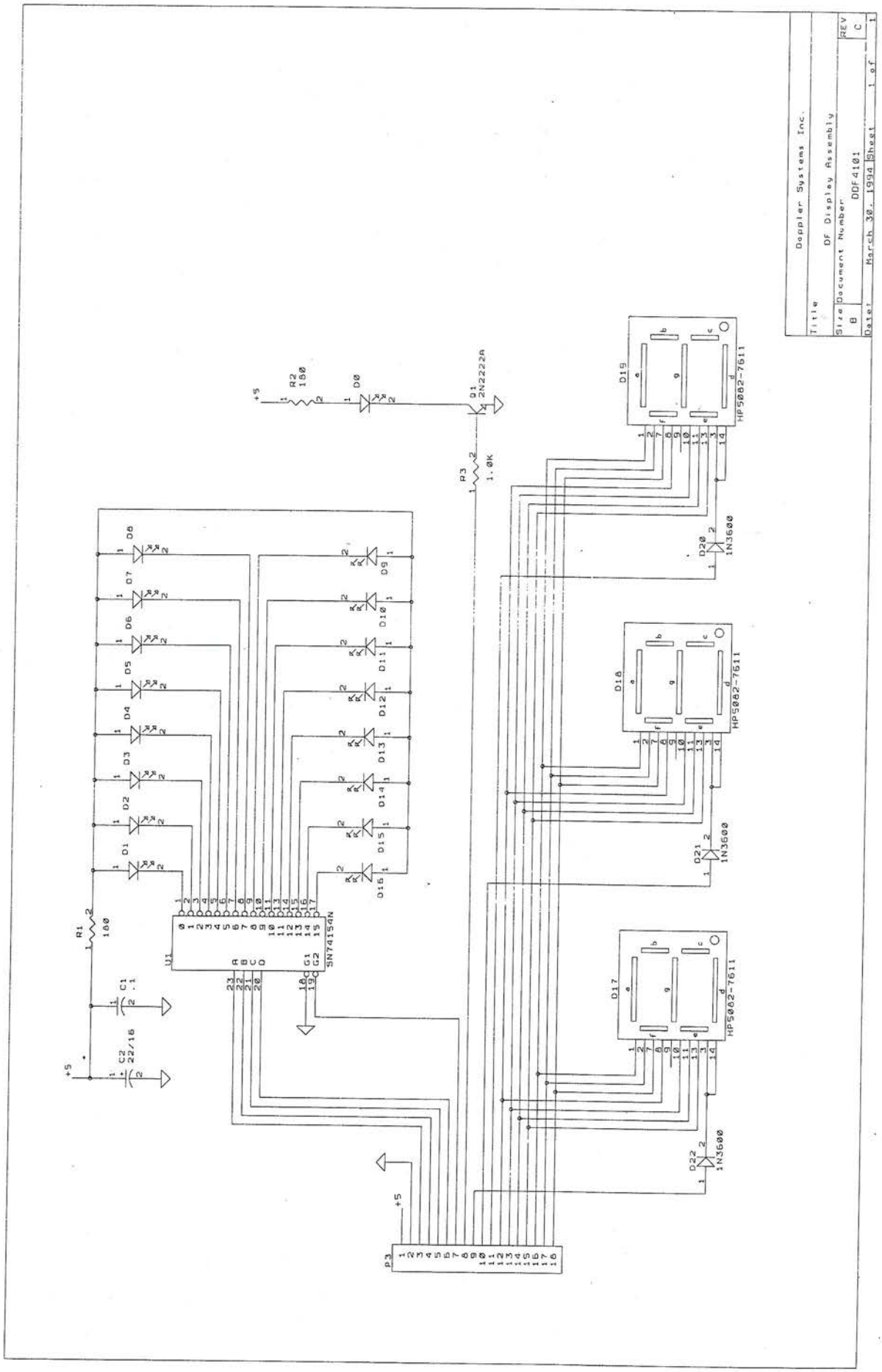
Inverters U2D and U2C translate the INT pulse train to +5 VDC for counter/display driver U3. The input on pin 13 of this IC overrides the internal display multiplex oscillator. The effect is to multiplex the display at a rate of 1200/4 = 300 Hz and to control the duty cycle (intensity) from RA.

If a display update does not occur for 6.8 seconds, binary counter U11 produces a high output which blanks the LED and digital displays. U11 is reset whenever a display update occurs. In the absence of such updates, it counts 1200 Hz pulses through gate U17D. After 8192 pulses are counted, its pin 3 output goes high and further counting stops. This inhibits the digital display via its scan input on pin 13. Blanking of the circular LEDs occurs on the 6.8 second time out and during the gate interval. U23C and U5D provide the required blanking signal to the LED decoder/driver on the Display board. If it is desired to hold the display indefinitely, the shorting plug at J9 can be moved from pin 3 to pin 1.

4.7 DISPLAY

Figure 4.7-1 shows the schematic of the Display board DDF4101 which is permanently connected to the Processor board DDF4102.

Figure 4.7-1


Doppler Systems Inc.
Title
DF Display Assembly
Size B
Document Number DDF4101
REV C
Date: March 30, 1994 Sheet 1 of 1
+5
R2 180
D0
Q1 2N2222A
R3 1.0K
D19
HPS082-7611
D20 1N3600
D18
HPS082-7611
D21 1N3600
D17
HPS082-7611
D22 1N3600
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
R1 100
C1 .1
C2 22/16
U1
SN74154N
P3

U1 is a 4 line to 16 line decoder capable of driving the 16 LEDs directly. An inhibit input on pin 19 blanks the display during the counting interval and after the 6.8 second time out period as discussed above.

Transistor Q1 drives the center ON LED from the intensity modulated 1200 Hz signal at K.

D17-D19 are high intensity 7-segment common anode displays multiplexed from U3 on the Processor board.

4.8 SERIAL INTERFACE

BCD bearing data from the digital display is serialized and an RS232C output generated for interfacing to a digital computer for data processing, recording, triangulation, etc. A single message consists of five ASCII characters: the hundreds digit, the tens digit, the units digit, a carriage return and a line feed. Each character contains a start bit, 7 or 8 data bits, an optional parity bit and a stop bit. The baud rate used is 300. It would require a maximum time of 11/300 = .037 seconds to send each character. The circuitry, however, sends a character every 1/18.75 = 0.053 seconds. A complete message of 5 characters would require 5/1.876 = 0.267 seconds. However, the message is initiated only when the display is updated. Since this occurs at a maximum rate of 1/1.875 = 0.533 seconds, ample time exists between characters and between messages to prevent overrunning.

Data from the digit display is available at the display multiplex rate of 300 digits per second. A first in-first out (FIFO) memory is used to temporarily hold the BCD display data in the proper order for the universal asynchronous receiver transmitter (UART) which performs the actual serialization. Loading of data into the FIFO follows the display multiplex sequence generated by the digit counter/driver on the Processor board: D3 (hundreds), D2 (tens) and D1 (units).

Figure 4.8-1 shows the schematic of the serial interface circuit. A positive leading edge on /ST causes flip flop U5B to set, starting the FIFO loading operation. The FIFO, U6, is reset and at the next falling edge of D1, the units digit multiplex pulse, flip flop U5A is set which in turn resets U5B. LOAD FIFO is now high and data present on the BCD lines (1's, 2's, 4's and 8's) is loaded into the FIFO on subsequent rising edges of D3, D2 and D1. The FIFO input is strobed by a leading edge on its pin 3. Following loading of all three digits, the trailing edge of D1 now resets U5B thereby ending the FIFO load sequence. When U5B is reset, it sets flip flop U3A which starts the FIFO unload sequence. UNLOAD FIFO goes high and 18.75 Hz pulses are gated to FIFO output shift pin 15. Data from the FIFO is passed through the quad and/or select

gate U4 and strobed into the UART by 18.75 Hz pulses shaped by differentiator U7F.

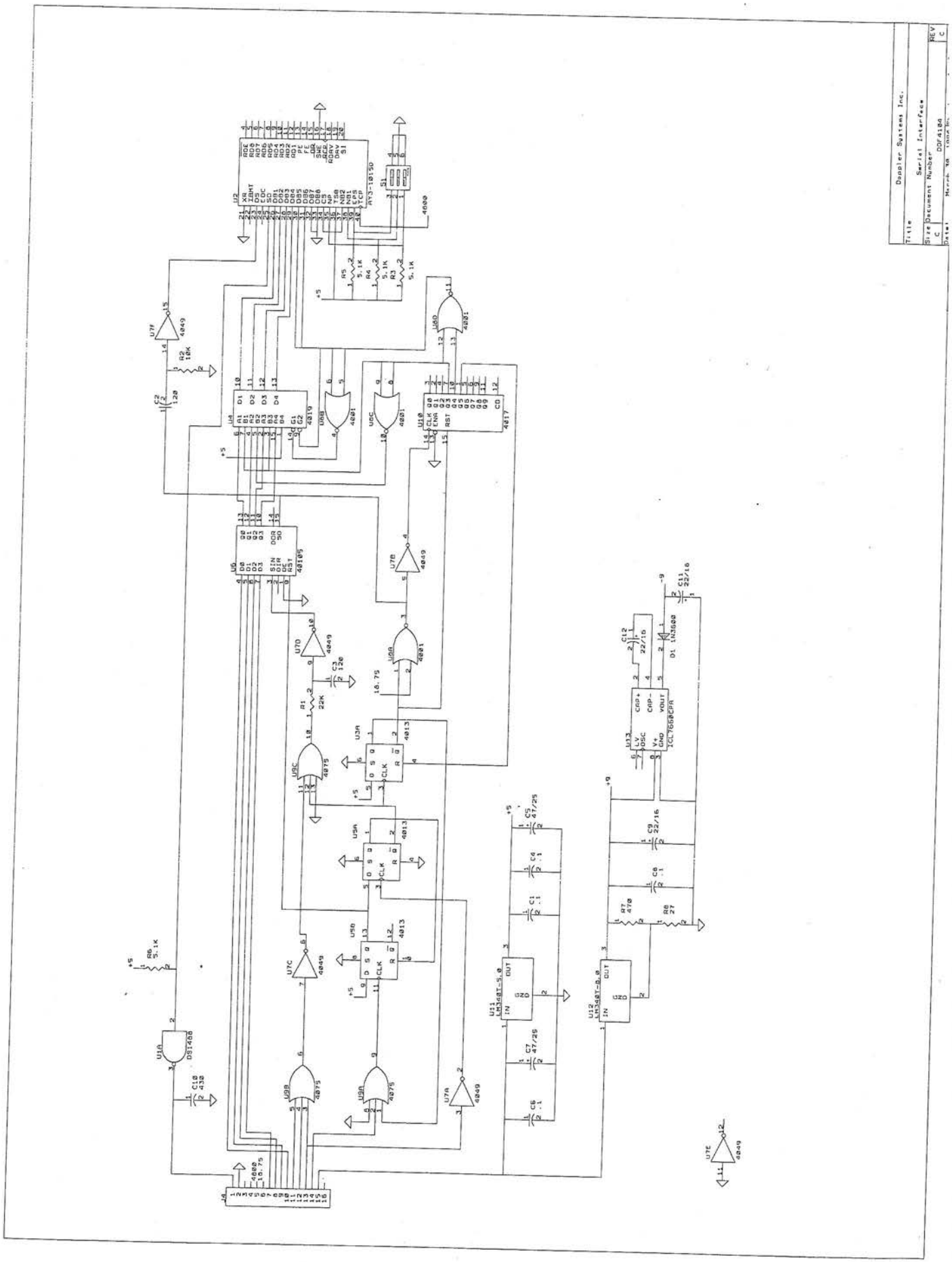
Decade counter U10 keeps track of the characters being sent to the UART. During the first 3 counts, (output 0, 1 and 2) the FIFO data is steered through U4 into the UART's four least significant bits. Most significant bits are 0, 0, 1, 1 so the full 8 bit UART input corresponds to the ASCII equivalent of the BCD digit transferred into the least significant bits. On counts 4 and 5, the UART input is connected to a binary value corresponding to ASCII <CR> and <LF> respectively. On count 6, the counter decodes an output which resets U3A thereby ending the FIFO unload sequence (and marking the end of the 5 character message.)

DIP switches S1-1, -2 and -3 can be set to program parity enable (on or off), parity sense (even or odd), and number of data bits transmitted (7 or 8).

The +5 VDC logic level output of the UART is translated to RS232C levels and inverted by U1.

The Serial Interface contains its own +5 VDC and +9 VDC linear voltage regulators U11 and U12. U13 is a switching type voltage converter that generates a -9 VDC for the RS232C logic low level.

Figure 4.8-1


Doppler Systems Inc.
Title
Serial Interface
Size
C
Document Number
DDF4104
REV
C
Date:
U2
AY3-1015D
S1
4000
R5 5.1K
R4 5.1K
R3 5.1K
+5
U7F
4049
R2 18K
C2 120
U4
4019
U8B
4001
U8C
4001
U8D
4001
U10
4017
U6
4018S
U7B
4049
U7D
4049
U7C
4049
U7A
4049
U7E
4049
U9B
4075
U9A
4075
U9C
4075
U9D
4013
U9A
4013
U9B
4013
U10
DS1488
C10 430
R6 5.1K
J6
4000
16.75
U70
4049
C3 120
R1 22K
16.75
U8A
4001
U13
ICL7660ECPA
C11 22/16
C12 22/16
D1 1N3600
C9 22/16
C8 .1
R7 470
R8 27
U11
LM340T-5.0
C5 47/25
C4 .1
C1 .1
C7 47/25
C6 .1
U12
LM340T-8.0

4.9 SPEECH SYNTHESIZER

Bearing data is enunciated every 2.13 seconds. Each digit is individually spoken as a "zero", "one", "two", etc. The timing associated with forming each word is internally determined by the synthesizer which contains its own 4.0 MHz crystal. Each digit in a given bearing is spoken at a fixed cadence of 8/18.75 = 0.427 seconds per digit. The entire 3 digit message then consumes 1.28 seconds, leaving 0.85 seconds of silence between messages. Since the display itself updates every 0.533 seconds, every fourth display will be enunciated (assuming continuous bearing updates from a prolonged carrier).

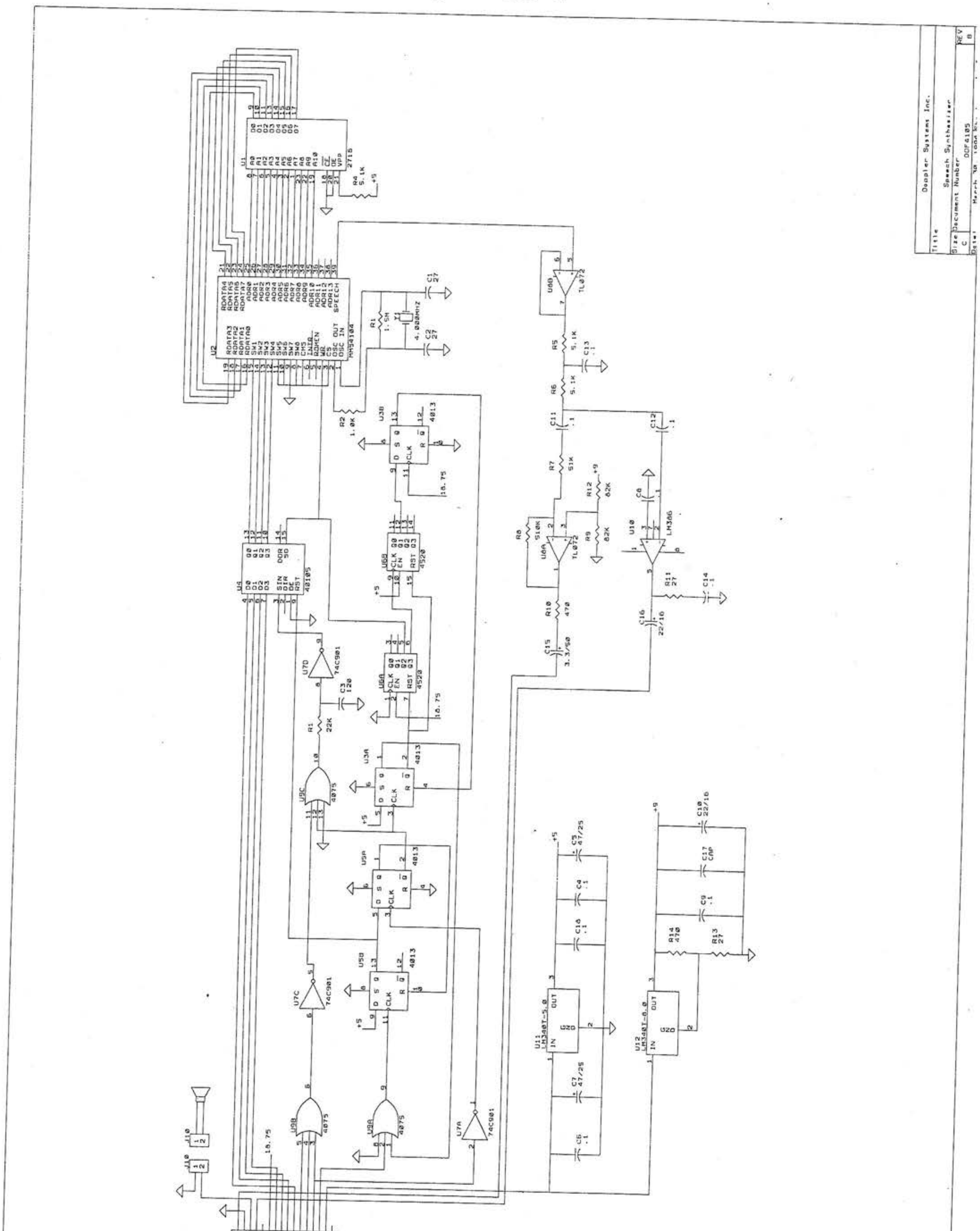
Data from the digit display is available at the display multiplex rate of 300 digits per second. A first in-first out (FIFO) memory is used to temporarily hold the BCD display data in the proper order for the speech synthesizer. Loading of data into the FIFO follows the display multiplex sequence generated by the digit counter/display on the Processor board: D3 (hundreds), D2 (tens) and D1 (units).

Figure 4.9-1 shows the schematic of the speech synthesis circuit. A positive leading edge on /ST causes flip/flop U5B to set, starting the FIFO loading operation. The FIFO, U6, is reset and at the next falling edge of D1, the units digit multiplex pulse, flip flop U5A is set which in turn resets U5B. LOAD FIFO is now high and data present on the BCD lines (1's, 2's, 4's and 8's) is loaded into the FIFO on subsequent rising edges of D3, D2 and D1. The FIFO input is strobed by a leading edge on its pin 3. Following loading of all three digits, the trailing edge of D1 now resets U5B thereby ending the FIFO load sequence. When U5B is reset, it sets flip flop U3A which starts the FIFO unload sequence. UNLOAD FIFO goes high and 18.75 Hz pulses are counted by synchronous binary counter U6A. A divide by 8 output of U6A causes data from the FIFO to shift out and be strobed into the synthesizer, U2, every 8/18.75 = 0.427 seconds. A second binary counter, U6B, together with flip flop U3B, generates an output after three digits have been synthesized. This marks the end of a message and resets U3.

Digitized speech is buffered by amplifier U8B and filtered to simulate a male voice. Amplifier U10 drives the internal loudspeaker through volume control RB. U8A is a fixed gain amplifier capable of driving a small 8 ohm external speaker such as used in an acoustic coupler. This permits external recording or telemetering of the bearing data from a remote site over a telephone line, radio link, etc.

The Speech Synthesizer contains its own linear voltage regulators, U11 and U12 to generate +5 and +9 VDC, respectively.

Figure 4.9-1



4.10 PARTS LISTS

Parts for each major assembly are listed below. Unless otherwise noted, all resistors are 1/4 watt, carbon composition, 5% tolerance. Mylar capacitors are 100 VDC, 10% tolerance and mica capacitors are 500 VDC, 5% tolerance. Disc ceramics are 50 VDC, +80, -20% tolerance.

PARTS LIST FOR DISPLAY BOARD, DDF4101

Ref	Item
U1	74154
R1	180 ohm
R2	180 ohm
R3	1 K
C1	.1 mf disc ceramic
C2	22 mf/16 VDC
Q1	2N2222A
D0-D16	BR3932S-H
D17-D19	HP 5082-7611
D20-22	1N3600

PARTS LIST FOR PROCESSOR BOARD DDF4102

Ref	Item	Ref	Item
U1	LM340T-5	R1	5.1 K
U2	CD4049	R2	10 M
U3	DDF49201	R3	10 K
U4	74LS193	R4	22 K
U5	CD4049	R5	22 K
U6	CD4001	R6	470 ohm
U7	LM340T-8	R7	27 ohm
U8	CD4071	R8	1 K
U9	CD4013	R9	1 K
U10	CD4520	R10	240 K
U11	CD4020	R11	180 K
U12	CD40103	R12	180 K
U13	LF347	R13	22 K
U14	TLO72	R14	51 K
U15	CD4017	R15	51 K
U16	CD4049	R16	27 K
U17	CD4071	R17	51 K
U18	CD4520	R18	240 K
U19	CD4018	R19	240 K
U20	LF347	R20	240 K
U21	CD4051	R21	27 K
U22	8-0.1 mf cap. ntwk.	R22	10 K
U23	CD4001	R23	51 K
U24	CD4013	R24	51 K
U25	CD4013	R25	51 K
U26	CD4066	R26	510 K
U27	NE570	R27	22 K

Ref	Item
R28	22 K
R29	51 K
R30	51 K
R31	10 M
R32	22 K
R33	22 K
R34	1.5 M
R35	470 ohm
R36	5.1 K
R38	5.1 K
R39	22 K
R40	10 K
R41	510 K
R42	820 K
R43	5.1 K
RA	100 K
RB	100 ohm
RC	100 K
C1	120 pf mica
C2	27 pf mica
C3	.1 mf disc ceramic
C4	100 mf/25 VDC
C5	.1 mf disc ceramic
C6	330 mf/10 VDC
C7	.01 mf mylar
C8	.1 mf disc ceramic
C9	220 mf/16 VDC
C10	120 pf mica
C11	22 mf/16 VDC
C12	.0047 mf mylar

Ref	Item
C13	.022 mf mylar
C14	.022 mf mylar
C15	.0047 mf mylar
C16	.0047 mf mylar
C17	.022 mf mylar
C18	.01 mf mylar
C19	120 pf mica
C20	.1 mf disc ceramic
C21	120 pf mica
C22	.022 mf mylar
C23	.0047 mf mylar
C24	.022 mf mylar
C25	.022 mf mylar
C26	.022 my mylar
C27	.1 mf disc ceramic
C28	220 mf/16 VDC
C29	3.3 mf/50 VDC
C30	1.0 mf/35 VDC tantalum
C31	3.3 mf/50 VDC
C32	27 pf mica
C33	1.0 mf/35 VDC tantalum
C34	1.0 mf/35 VDC tantalum
C35	.001 mf disc ceramic
Y1	1.7280 MHz
F1	2 amp.
CR1	1N3600
CR2	1N3600

PARTS LIST FOR RF SUMMER BOARD, DDF4103

Ref	Item
U1-U4	MWA110
R1-R2	240 ohm
R3-R6	33 ohm
R7-R8	240 ohm
R9-R12	1000 ohm
C1-C12	.001 mf disc ceramic
L1-L4	1000 uH RFC

PARTS LIST FOR SERIAL INTERFACE BOARD, DDF4104

Ref	Item	Ref	Item
U1	DF1488	R5	5.1 K
U2	AY-3-1015D	R6	5.1 K
U3	CD4013	R7	470 ohm
U4	CD4019	R8	27 ohm
U5	CD4013	C1	.1 mf disc ceramic
U6	CD40105	C2	120 pf mica
U7	CD4049	C3	120 pf mica
U8	CD4001	C4	.1 mf disc ceramic
U9	CD4075	C5	47 mf/25 VDC
U10	CD4017	C6	.1 mf disc ceramic
U11	LM340T-5	C7	47 mf/25 VDC
U12	LM340T-8	C8	.1 mf disc ceramic
U13	ICL7660	C9	22 mf/16 VDC
R1	22 K	C10	430 pf mica
R2	10 K	C11	22 mf/16 VDC
R3	5.1 K	C12	22 mf/16 VDC
R4	5.1 K	CR1	1N3600

PARTS LIST FOR SPEECH SYNTHESIZER BOARD, DDF4105

Ref	Item	Ref	Item
U1	MM2716/DDF4212	C1	27 pf mica
U2	MM54104	C2	27 pf mica
U3	CD4013	C3	120 pf mica
U4	CD40105	C4	.1 mf disc ceramic
U5	CD4013	C5	47 mf/25 VDC
U6	CD4520	C6	47 mf/25 VDC
U7	74C901	C7	.1 mf disc ceramic
U8	TL072	C8	.1 mf disc ceramic
U9	CD4075	C9	.1 mf disc ceramic
U10	LM386	C10	22 mf/16 VDC
U11	LM340T-5	C11	.1 mf disc ceramic
U12	LM340T-8	C12	.1 mf disc ceramic
R1	1.5 M	C13	.1 mf disc ceramic
R2	1.0 K	C14	.1 mf disc ceramic
R3	22 K	C15	3.3 mf/50 VDC
R4	5.1 K	C16	22 mf/16 VDC
R5	5.1 K	C17	.1 mf disc ceramic
R6	5.1 K	C18	.1 mf disc ceramic
R7	51 K	Y1	4.000 MHz
R8	510 K		
R9	82 K		
R10	470 ohm		
R11	27 ohm		
R12	82 K		
R13	27 ohm		
R14	470 ohm		

Section 5.0
SPECIFICATIONS (TYPICAL)

1.0 System Performance	
1.1Type	Quasi-Doppler, continuous commutation of four antennas
1.2 Antenna commutation frequency	300 Hz
1.3 Frequency Range	52 to 500 MHz
1.4 Accuracy	+/-5 degrees at 150 MHz, +/- 25 degrees at 480 MHz
1.5 RF pulse duration	150 milliseconds minimum
2.0 RF circuit	
2.1 RF power gain	8 dB at 150 MHz, 2 dB at 150 MHz, 0.5 dB at 480 MHz
2.2 Noise figure	5.0
2.3 Input and output impedances	50 ohms
2.4 Interface	BNC connectors to antennas and receiver on back panel
3.0 Audio Input	
3.1 Input level	10 mVRMS to 2.0 VRMS (automatic level control provided)
3.2 Input impedance	5.0K minimum
3.3 Display trigger	Audio squelch (normal) or external mute (via optional jumper)
3.4 Mute voltage	+5 to +9 VDC
3.5 Mute input impedance	1.0 M minimum
3.6 Interface	15 pin subminiature D connector on back panel; mating connector and cover supplied
4.0 Display	
4.1 Bearing Display	16 LEDs in circular pattern, all models; 3 digit degree readout, models 4002-4004
4.2 Display intensity	Adjustable from front panel control
4.3 Display update rate	1.875 updates per second
4.4 Display hold time	Either 6.8 seconds or indefinite by jumper selection
5.0 Serial Data Output (Model 4003 only)	
5.1 Output data	Bearing in degrees (hundreds - tens - units - {CR} - {LF})
5.2 Format	ASCII with 7 or 8 data bits, even or odd parity, parity on or off (switch selectable)

5.3 Timing	300 Baud message sent every 0.533 - seconds
5.4 Voltage levels	RS232C compatible
5.5 Interface	15 pin subminiature D connector on back panel
6.0 Speech Output (Model 4004 only)	
6.1 Synthesized message	Bearing in degrees: "hundreds-tens-units"
6.2 Format	Each digit individually spoken as "zero", "one", etc.
6.3 Timing	Message spoken every 2.13 seconds
6.4 Output level	Adjustable from front panel control
6.5 Auxiliary output	Fixed level output capable of driving external 8 ohm speaker for acoustical coupling to telephone, tape recorder, etc.
6.6 Interface	15 pin subminiature D connector on back panel
7.0 Power	
7.1 Input voltage	11.5 to 13.5 VDC
7.2 Input current	0.5 amperes fused internally at 2.0 amps
7.3 Interface	15 pin subminiature D connector or back panel
8.0 Mechanical	
8.1 Mounting	Mounting bracket supplied for under dash mounting.
8.2 Size	3.6H x 5.5W x 8.9D inches excluding mounting bracket
8.3 Weight	1.0 pound
9.0 Operating Temperature	0 to 50 degrees C