AN3432
Application note

How to choose a bypass diode for a silicon panel junction box

Introduction

Today, the main technologies used in solar panel are polycrystalline and mono crystalline silicon solar cells. When one solar cell of the panel is shaded while the others are illuminated, a hot spot could appear and leads to the shaded cell destruction. The bypass diode is an efficient solution to eliminate the “hot spot” and maintain the current delivery. The Schottky diode is a cost effective candidate. Its V_{RRM}, V_F/I_R trade off need to fit the panel and junction box characteristics.

This document gives a method to select the most appropriate diode versus the panel characteristics.

Contents

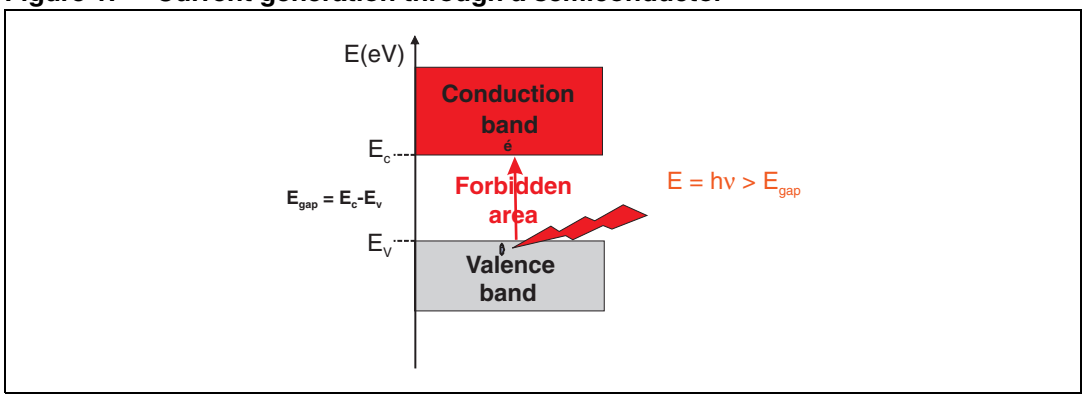
1 Photocurrent production basics of silicon solar cells

1.1 The photovoltaic effect

To generate a current through a semi conductor, some energy is required to extract the electron from the valence band to the conduction band. This energy is greater than material band gap energy (E_{gap}).

Thus in case of silicon solar cell, if the photon energy (sunlight carrier) E = hν is higher than the silicon band gap energy E_{gap} =1.12eV, the electrons migrate through a PN junction.

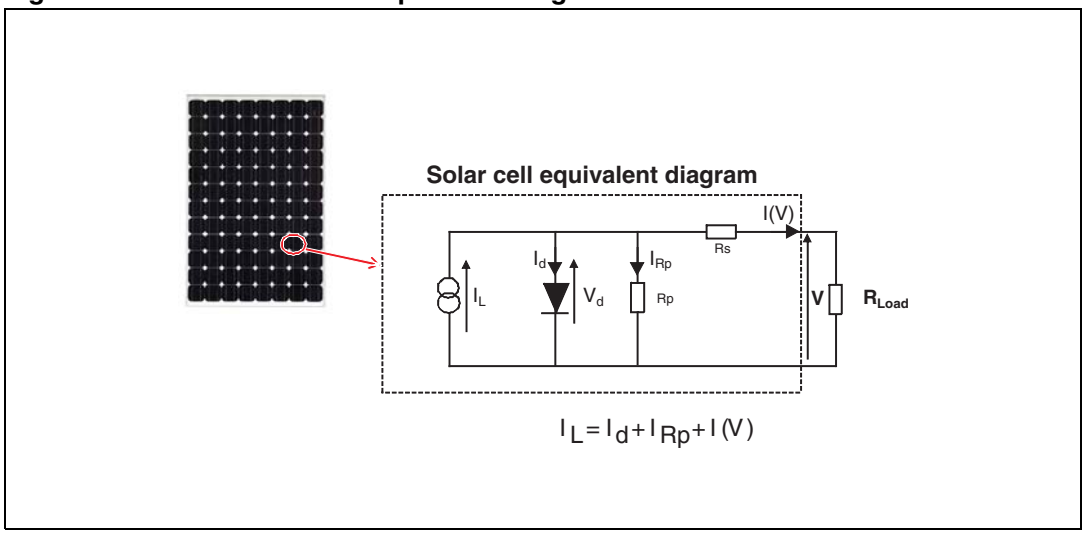
Figure 1. Current generation through a semiconductor



1.2 The solar cell model

Silicon solar cell creates a photocurrent called I_L that is proportional to illumination and independent of output cell voltage. However, when this voltage increases, a part of this current is dissipated in p-n junction. This is why the equivalent model, shown in *Figure 2*, consists in a current generator (photocurrent), a diode (intrinsic p-n junction), two resistances R_p (parallel resistance: models the noise current between top and bottom of the solar cell) and R_s (series resistance: simulates the materials and contact losses).

Figure 2. Silicon solar cell equivalent diagram



The circuit model shown on *Figure 2* gives the solar cell current (I(V)) versus the solar cell output voltage (V)

Equation 1

$$I(V) = I_L - I_0 \left(\exp\left[\frac{q(V + I(V)\cdot R_s)}{KT}\right] - 1\right) - \frac{(V + I(V)\cdot R_s)}{R_p}$$

Where:

I_0 is the reverse bias saturation current, depending on cell die and junction characteristics

K is the Boltzmann constant: $1.38.10^{-23}$

q is the electron charge $1.602.10^{-19}$ C

T is the temperature in K

1.3 Main parameters of solar cells

1.3.1 Short circuit current (I_{sc}) and open circuit voltage (V_{oc})

The solar cells or panel are usually characterized by their short circuit current (I_{sc}) and their open circuit voltage (V_{oc}).

The short circuit current (I_{sc}) is the current generated by the solar cell or panel when output voltage of the cell or panel is set to 0 V.

Equation 2

$$I_L = I_{sc} + I_{sc} \cdot \frac{R_s}{R_p} + I_o \cdot \left(\exp\left(\frac{q}{KT} \cdot I_{sc} \cdot R_s\right) - 1\right)$$

R_S/R_P and R_S being negligible, the short circuit current is close to the photocurrent I_L generated by the cell and is the maximum possible current generated by the cell for a fixed illumination.

Equation 3

$$I_{sc} \sim I_L$$

The open circuit voltage (V_{oc}) is the voltage corresponding to the output current of solar cell or panel set to 0. The photocurrent is equal to the current lost in the intrinsic element of the cell, and V_{oc} is equal to the intrinsic diode forward voltage (V_d).

Equation 4

$$I_L = I_O \cdot (\exp(\frac{q}{KT} \cdot V_{oc}) - 1) - \frac{V_{oc}}{R_p}$$

Equation 5

$$V_{oc} = V_d$$

In the following, for easier the reading, V_{oc} is the open circuit voltage of the panel and V_{oc_u} the open circuit voltage of the solar cell. The relation between them is given in *Equation 6*.

Equation 6

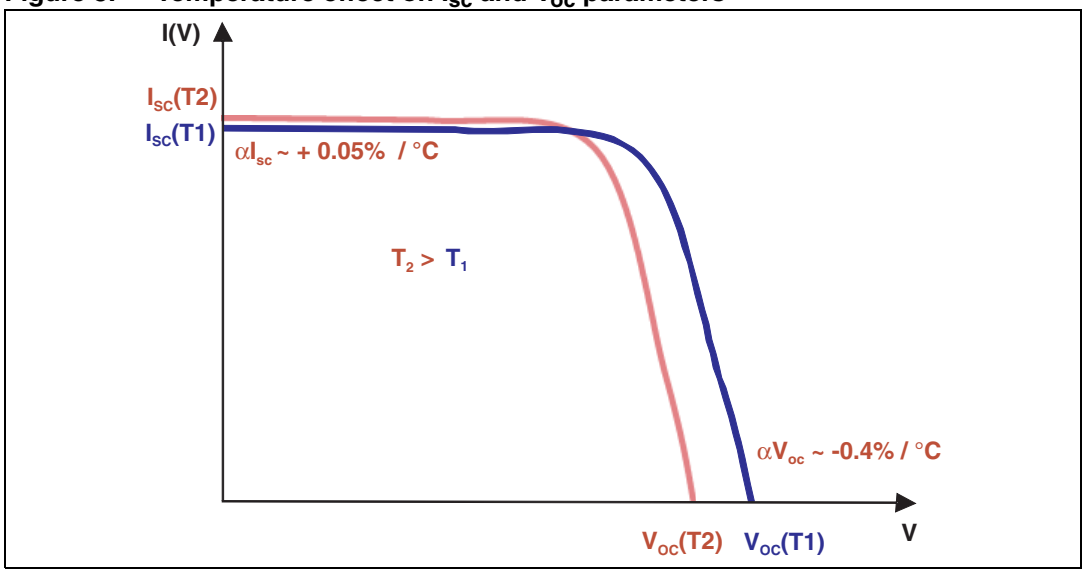
$$V_{oc} = \sum_{i=1}^{nb} V_{oc\_u\_i}$$

where nb is the number of cells contained in one panel.

1.3.2 V_{oc} and I_{sc} variations with ambient temperature

The open circuit voltage is mainly linked with the parasitic diode forward voltage then it is temperature dependent with a negative temperature coefficient (αV_{oc}). Then the maximum value for V_{oc} is the value at minimum junction temperature specified in the panel data sheet. Strongly linked with the photocurrent, the short circuit current increases slightly with the temperature (αI_{sc}>0).

Figure 3. Temperature effect on I_{sc} and V_{oc} parameters



Considering the example of a 190 W solar panel. In standard test conditions (STC) @T_{amb} = 25 °C, V_{oc} = 33 V, I_{sc} = 7.89 A:

αI_{sc} = 0.05%/°C; αV_{oc} = -0.4%/°C at an operating temperature range of -40 °C, 85 °C.

$$V_{oc}(-40\ °C) = 33 + \left[\frac{33 \cdot -0.4}{100} \cdot (-40\ -25)\right]$$

$V_{oc}(-40\ °C) = V_{oc}max = 41.6$ V

That is, the V_{oc} deviation is 26% versus V_{oc} (STC)

$$I_{sc}(85\ °C) = 7.89 + \frac{7.89 \cdot 0.05}{100} \cdot (85 - 25)$$

$I_{sc}(85\ °C) = I_{sc}max = 8.13$ A

Then, I_{sc} max is 3% higher than I_{sc} (STC)

1.4 Hot spot phenomenon

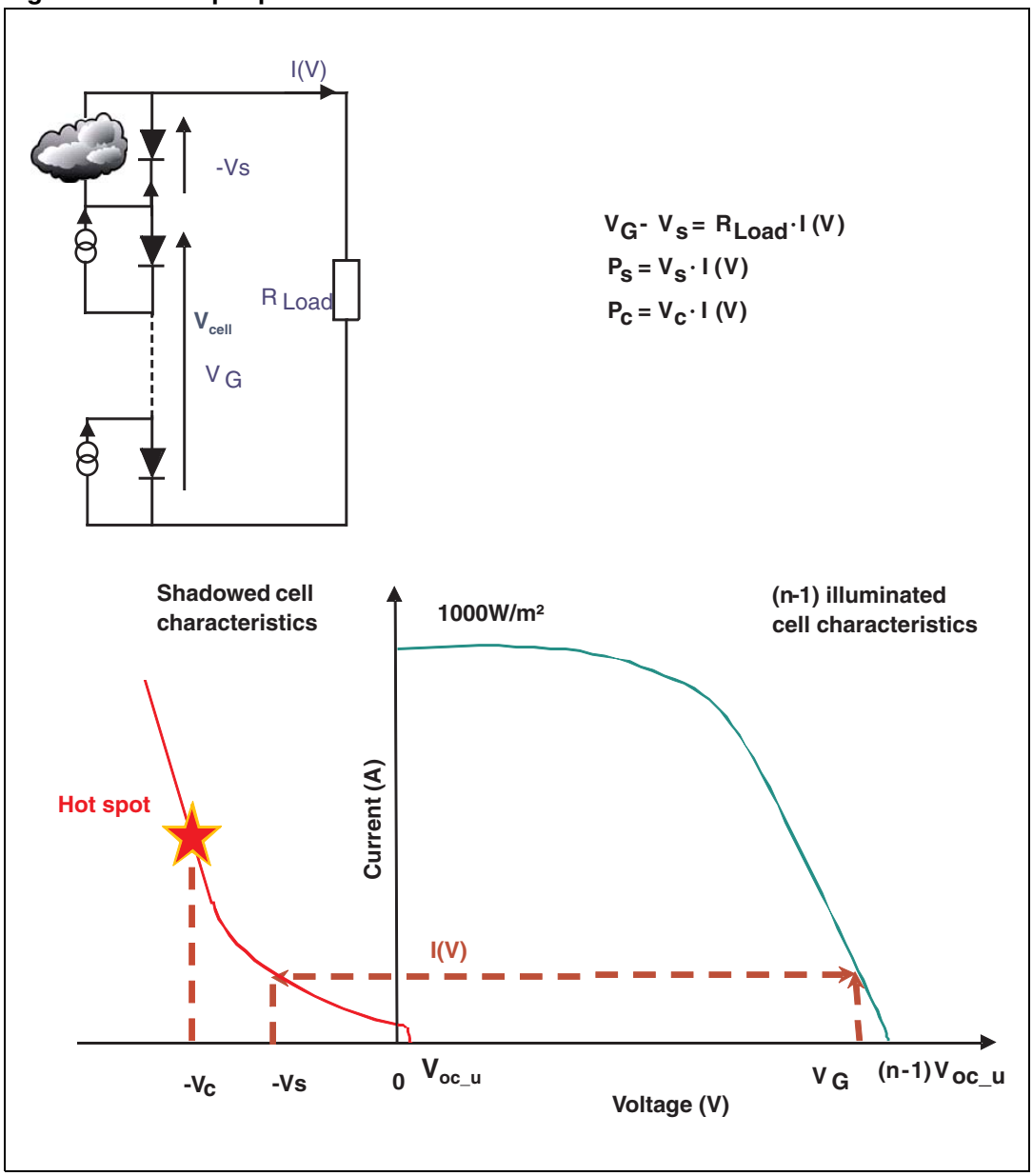
The hot spot phenomenon happens when one cell of the panel is shaded while the others are illuminated, and when this shaded cell is not able to exhaust its generated power dissipation.

The shaded cell behaves as a diode polarized in reverse and generates reverse power P_s. The other cells generate a current that flows through the shaded cell and the load R_{load}.

Any solar cell has its own critical power dissipation P_c that must not be exceeded and depends on its cooling and material structures, its area, its maximum operating temperature and ambient temperature. A shaded cell may be destroyed when its reverse dissipation exceeds P_c. This is the hot spot.

The manufacturers usually define a breakdown voltage V_c. Its value depends on the solar cell technology (poly-silicon or mono-silicon) and the manufacturing process.

Figure 4. Hot spot phenomenon



There is no risk of hot spot while:

Equation 7

$P_s < P_c$

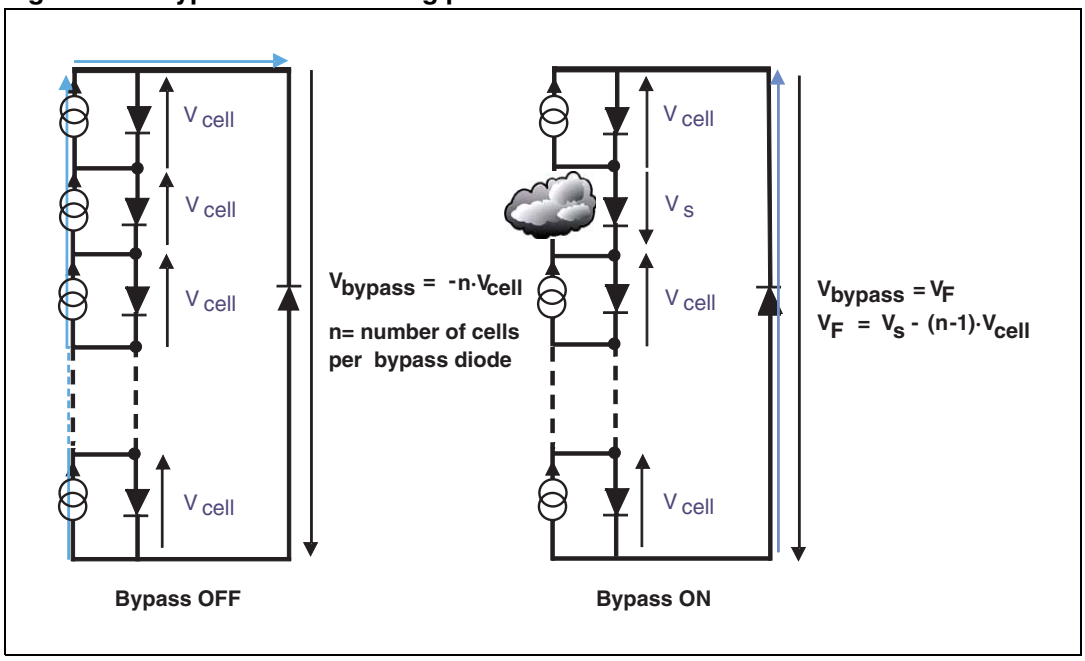
To eliminate the hot spot phenomenon, a dedicated circuit should bypass the partially shaded module and eventually it should maintain the operation of the other PV modules creating a path for their current.

2 Bypass diode inside the junction box

2.1 Bypass function

The bypass diode principle is to use a diode in reverse paralleling with several solar cells (see *Figure 5*). The bypass diode is blocked when all cells are illuminated, and conducts when one or several cells are shadowed.

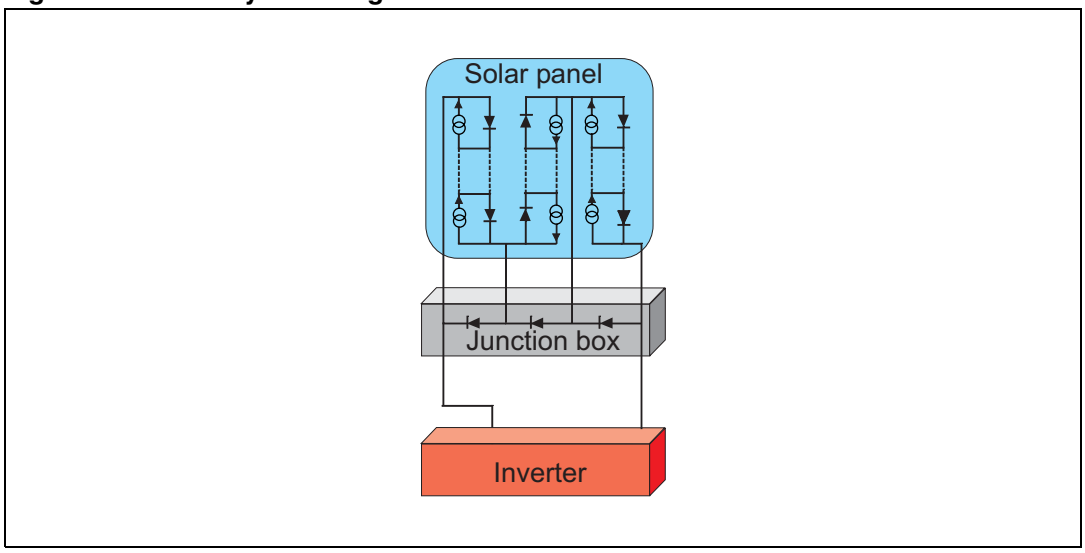
Figure 5. Bypass diode working phases



2.2 Junction box

Bypass diodes are rarely mounted directly on the solar panel. They are soldered in a so called junction box that is placed at the rear of the solar panel. Most of the time, it contains three diodes in series as explained in paragraph 2.3.1. The junction box design has a significant impact on the thermal diode performance. When qualified without solar module, the junction box has to meet DIN V VDE V 0126-5:2008 standard requirements. When qualified with its solar module, the standard is EN61215.

Figure 6. Solar system diagram



Ideally, a bypass diode should have a forward voltage (V_F) and a leakage current (I_R) as low as possible. However, these are conflicting objectives. Special care needs to be taken to eliminate any risk of thermal runaway.

The junction box manufacturers use Schottky diode for its low forward voltage. The choice of maximum reverse voltage is made versus the number and voltage of the solar cells in series. Then the trade off “conduction voltage V_F/reverse current I_R” is selected according to the total power losses ratings.

2.3 V_{RRM} is the first rating criterion

The maximum repetitive reverse voltage (V_{RRM}) of the bypass diode is directly linked with the number of cells bridged by the bypass diode.

2.3.1 Maximum number of solar cells to bridge with bypass

The maximum number of cells to bridge is defined by the breakdown voltage (V_c). The literature gives breakdown voltage (V_c) range for the poly-silicon cells from 12 V to 20 V. For mono-silicon cells the breakdown voltage extends up to 30 V.

For an efficient operation, there are two conditions to fulfill:

- Bypass diode has to conduct when one cell is shadowed.
- The shadowed cell voltage V_s must stay under its breakdown voltage (V_c). It is defined by the cell manufacturer and is the minimum value of the manufacturing distribution.

The maximum number of solar cells (n_{max}) to bridge is calculated using both these conditions:

Equation 8

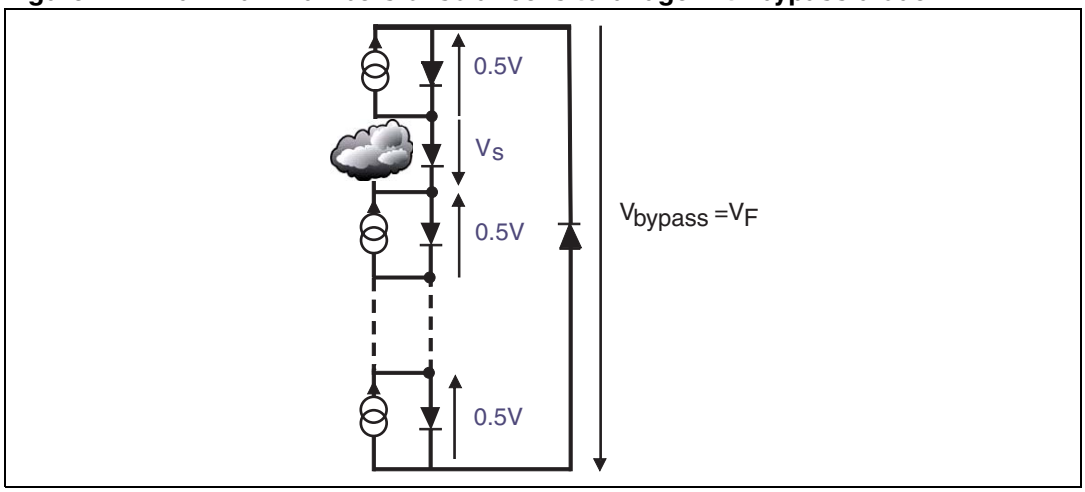
$$V_{bypass} = V_s - (n-1) \cdot V_{oc\_u}$$

With $V_s < V_c$ $V_{oc\_u} \approx 0.5\ V$ $V_{bypass} = V_F$

$$V_F < V_c - (n_{max} - 1) \cdot 0.5$$

$$n_{max} < \frac{V_c - V_F}{0.5} + 1$$

Figure 7. Maximum numbers of solar cells to bridge with bypass diode



Considering poly-silicon solar cells with a breakdown voltage V_c of 12 V and a bypass diode forward voltage V_F of 0.5 V, the maximum number n_{max} of solar cells bridged by the bypass diode is 24. This is the common setting used by module manufacturers.

2.3.2 V_{RRM} of bypass diode

Knowing the number of bypass diodes nd and the V_{oc} of the panel, the maximum repetitive reverse voltage (V_{RRM}) of the bypass diode can be calculated. In the worst case, the bypass diode reverse voltage is equal to the open circuit voltage (V_{oc_max}) of the solar panel divided by the number of bypass diodes nd. V_{oc_max} is the open circuit voltage at the minimum ambient temperature with the maximum irradiance.

Equation 9

$$V_{oc}max = V_{oc}(T_{jmin}) \cdot (1 + dt\%)$$

$$V_{RRM} > \frac{V_{oc}max}{nd}$$

where dt% = average voltage dispersion, which depends on the panel manufacturer.

Most of the time, the junction box manufacturer is different from the solar panel manufacturer. Then the junction box is not dedicated to one panel, but it could be used with any solar panel power range up to 400 W.

For a 400 W panel with a total V_{oc} of 85 V in STC, its highest voltage is V_{oc} (-40°C) = 107 V (see *Section 1.3.2*). If the deviation tolerance dt% is 20% (average dispersion estimate given in the literature) and 3 bypass diodes are used in the junction box, the reverse voltage of each bypass diode is 43 V, then V = 45 V is selected.

This is probably the reason why the diode with a V_{RRM} = 45 V is the most widely used in the junction boxes.

3 Application constraints

3.1 Constraints linked with the junction box characteristics

The forward voltage induces conduction losses (P_{cond}) and leakage current induces reverse losses (P_{rev}). The best trade off needs to take into account:

- Solar panel efficiency impact
- Thermal runaway risk (directly linked with power losses)
- Compatibility with flash test
- Thermal test (linked with forward voltage)
- Thermal cycling test

3.1.1 Power losses

Diode conduction losses

When the diode is conducting in DC mode, its forward voltage causes power losses called P_{cond}. These losses represent the most part of the total power losses and decrease when the junction temperature increases. The application note AN604 describes the way to calculate them:

Equation 10

$$P_{cond}(T_j) = V_F(I_F, T_j) \cdot I_F \qquad I_F = I_{PM} - I_S$$

Considering a solar panel built with 48 cells in series, divided in two sets of 24 cells protected by one bypass diode each. If one cell of the first set is shadowed while the other 47 cells are fully illuminated, the bypass diode of the shadowed set is conducting, and the bypass diode of the second set is in reverse bias. The second set generates a current I_{pm} while the first set sinks the reverse current I_s of the shaded cell. Then the conduction losses are:

Equation 11

$$P_{cond}max(T_j) = V_F(I_{pm} - I_s, T_j) \cdot (I_{pm} - I_s)$$

The maximum loss calculations are made with the current through the bypass diode equal to the maximum photocurrent I_{SC}.

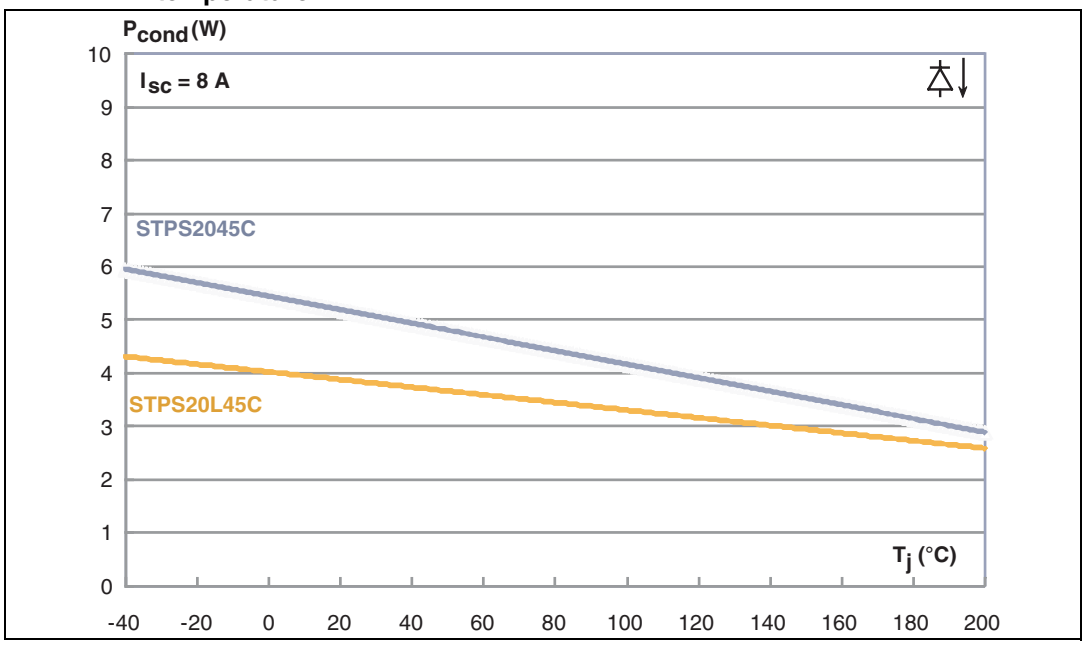
Equation 12

$$P_{cond}(T_j) \leq V_F(I_{sc}, T_j) \cdot (I_{sc})$$

Figure 8 shows the maximum conduction losses for two different types of diodes:

- STPS20L45 (low forward voltage)
- STPS2045 (lower leakage current and higher forward voltage than STPS2045)

Figure 8. STPS20L45C and STPS2045C conduction losses versus junction temperature



For a first consideration the lower is the forward voltage the higher is the efficiency. However, for a Schottky diode, a lower forward voltage causes a higher leakage current. This is its main technological trade off.

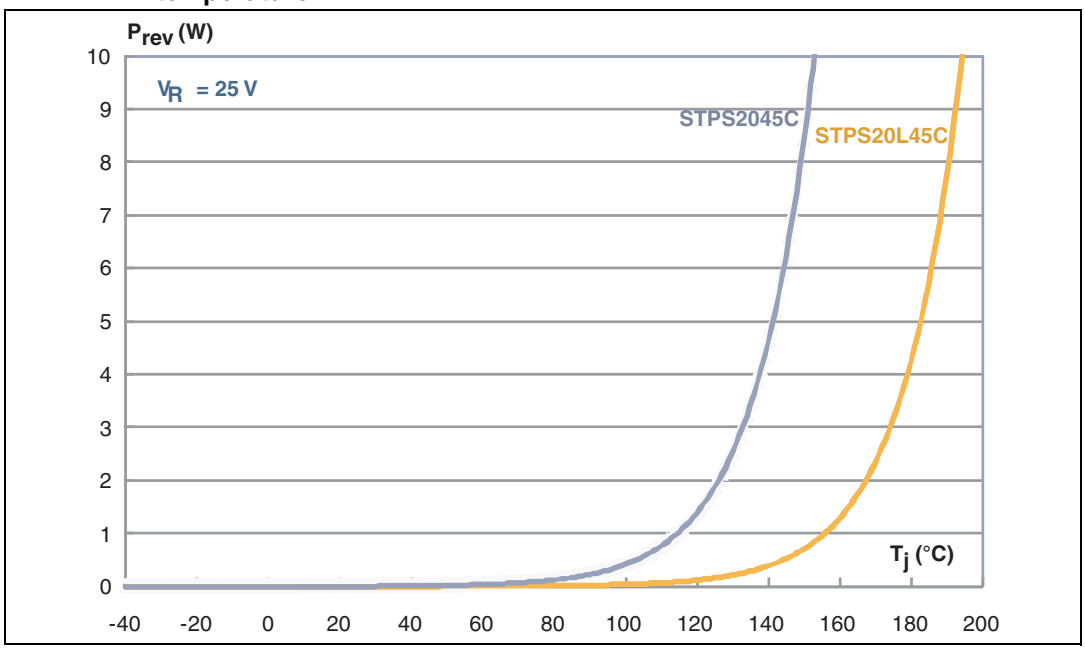
Diode reverse losses

When the diode is reversed bias, all the cells bridged by the diode generate photocurrent. Most of the time, in bypass application, the leakage current induces reverse losses. They increase with the junction temperature and can be calculated using *Equation 13*.

Equation 13

$$P_{rev}(T_j) = V_R \cdot I_R(V_R, 125°C) \cdot e^{c(Tj-125°C)}$$

Figure 9. STPS20L45C and STPS2045C reverse losses versus junction temperature



The reverse losses curves, shown in *Figure 9*, are calculated in the following application conditions:

P_{panel} = 400 W at T_{amb} = 85 °C, 3 bypass diodes, $V_{OC(STC)}$ = 85 V

To calculate the maximum reverse voltage V_{RRM}, use the method described in *Section 2.3.2*.

V_R = 25 V, $T_j = T_{amb}$

P_{rev_2045}(85 °C) = 0.014 W

P_{rev_20L45}(85 °C) = 0.13 W

In application conditions, the solar module efficiency lost due to bypass diodes is around 0.05% for STPS20L45 and 0.004% for STPS2045.

The diode with the lower forward voltage (STPS20L45C) has the drawback of a higher leakage current. The consequence is not visible on power module efficiency due to the low level contribution of the bypass diode reverse losses.

However, it impacts the diode choice since the leakage current is directly linked with thermal runaway risk. To avoid this phenomenon the choice of a diode with higher forward voltage is mandatory as described in *Section 3.1.2*.

3.1.2 Thermal runaway risk

The thermal runaway results in the loss of temperature control, due to the inability to exhaust the power losses generated by the diode operation.

In the bypass diode application, the most critical case is when the diode conducts and suddenly turns off. At this specific time t_0 the following rule is applied to eliminate thermal runaway risk:

Equation 14

$$P_{cond}(T_{j@to}) > P_{rev}(T_{j@to})$$

The junction temperature depends on the junction box thermal resistance between ambient temperature (T_a) and diode case temperature (T_c) and the thermal resistance between the diode junction and the diode case, given in the diode datasheet as the $R_{th(j-c)}$ parameter. The power losses and these parameters are linked by the thermal law.

Equation 15

$$P_{Thermal}(T_j) = \frac{(T_j - T_a)}{R_{th(j-c)} + R_{th(c-a)}}$$

and

$$P_{cond}(T_{j@to}) = P_{Thermal}(T_{j@to})$$

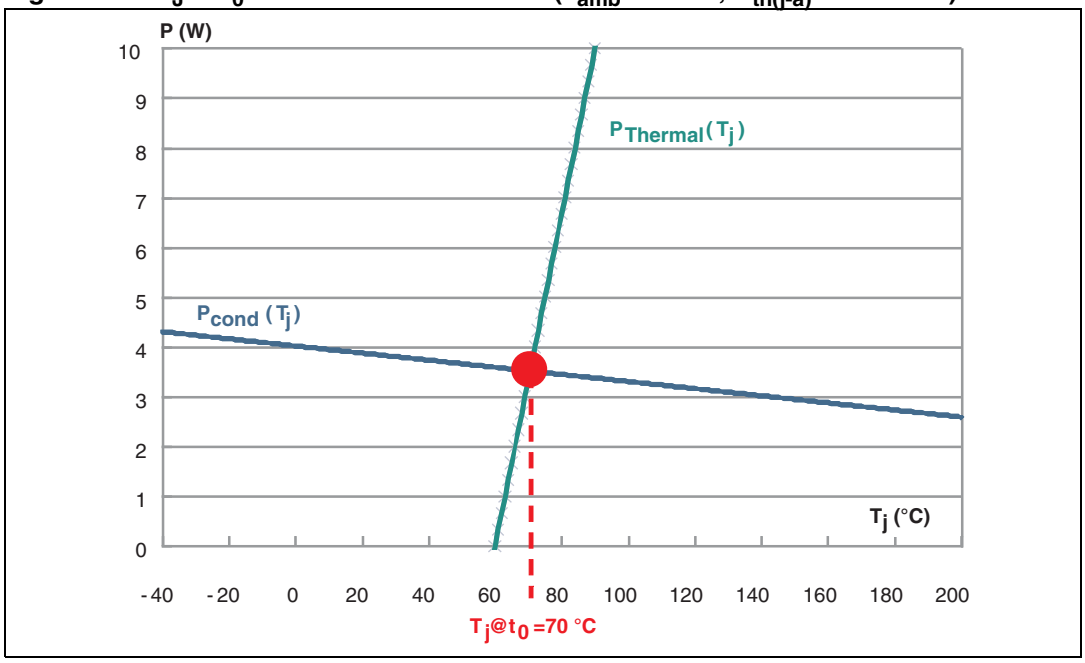
The conduction losses are given by:

Equation 16

$$P_{cond}(T_j) = V_F(I_{sc}, T_j) \cdot I_{sc}$$

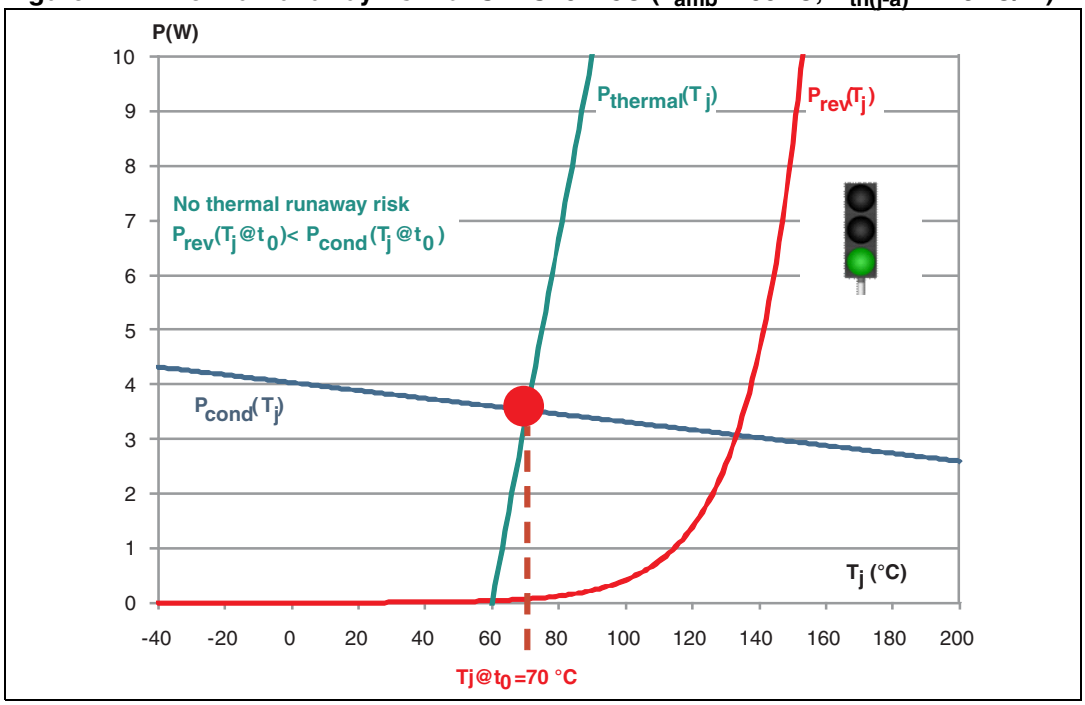
A graphical interpretation is presented in *Figure 10* with STPS20L45C diode, the current is 8 A, the ambient temperature is 60 °C, $R_{th(c-a)}$ = 3 °C/W, $R_{th(j-c)}$ = 1.3 °C/W. The green curve is the heat power that the junction can dissipate. The blue curve is the conduction losses generated by the diode. The curves cross point gives the junction temperature at the specific time t_0. In this condition, the junction temperature $T_{j@t0}$ = 70 °C is shown in *Figure 10*.

Figure 10. T_J @ t_0 in case of STPS20L45C (T_{amb} = 60 °C, $R_{th(j-a)}$ = 4.3 °C/W)



By adding the reverse losses curve on the chart, *Equation 14* is respected.

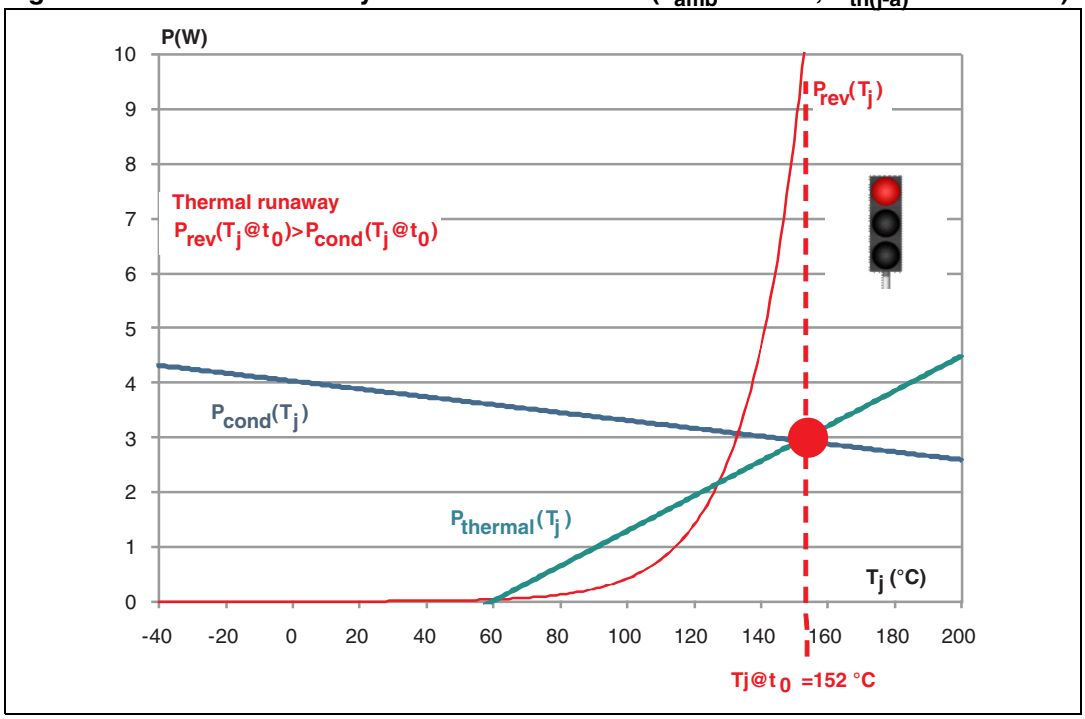
Figure 11. Thermal runaway risk for STPS20L45C (T_{amb} = 60 °C, $R_{th(j-a)}$ = 4.3 °C/W)



As shown in *Figure 11*, there is no risk of thermal runaway since the operation of the diode moves from the blue curve to the red curve then slips to thermal equilibrium close to the ambient temperature (60 °C)

In another example, if the junction box presents a $R_{th(c-a)}$ = 30 °C/W, with an ambient temperature around 85 °C, there is a risk of thermal runaway as shown in *Figure 12*.

Figure 12. Thermal runaway risk for STPS20L45C (T_{amb} = 85 °C, $R_{th(j-a)}$ = 31.3 °C/W)



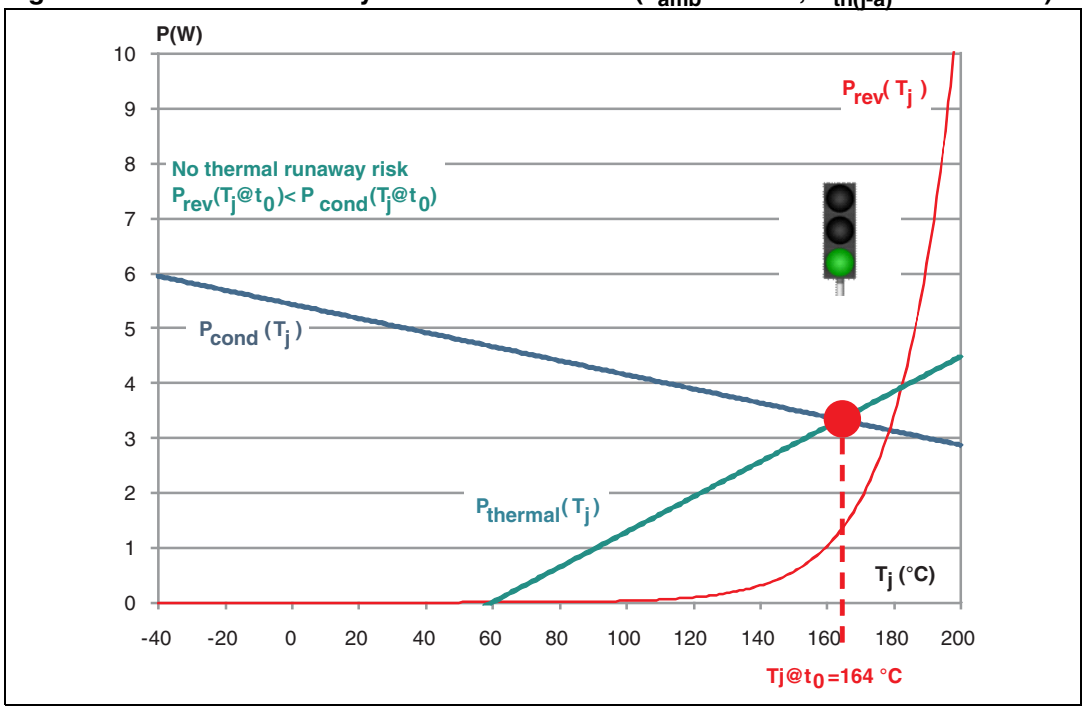
As shown on *Figure 12*, the junction temperature is 152°C in conduction. At turn-off this temperature would generate initial losses of 9.5 W making the equilibrium point impossible since both temperature and leakage will increase in a thermal runaway manner due to the poor cooling.

To solve this problem, there are two options:

Reduce the thermal resistance $R_{th(c-a)}$ of the junction box (modify geometry, change compound…)

Select a diode with much less leakage current as STPS2045C, as shown in *Figure 13*, even if the junction temperature at turn off is higher than STPS20L45 due to its higher forward voltage drop and power losses. Therefore, there is no thermal runaway risk anymore.

Figure 13. Thermal runaway risk for STPS2045C (T_{amb} = 85 °C, $R_{th(j-a)}$ = 31.3 °C/W)

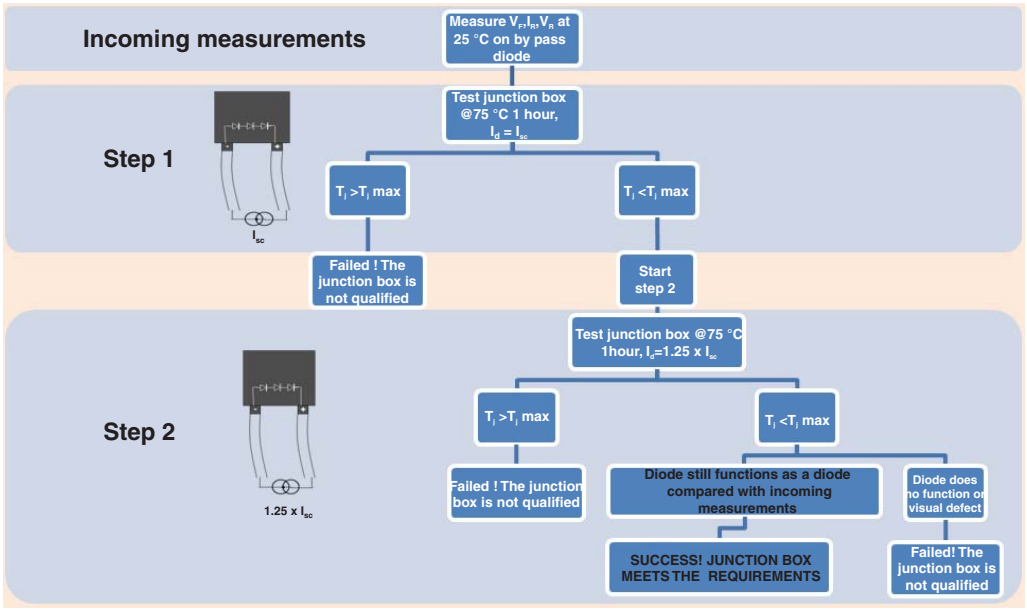


3.2 Constraints linked with reliability test

3.2.1 Thermal test

This test is defined in EN61215 and in DIN V VDE V 0126-5:2008 in two steps as described in *Figure 14*.

Figure 14. Thermal test synopsis



Using *Equation 17* and *Equation 18* it is possible to evaluate if the requirements of EN61215 can be met.

Equation 17

$$P_{cond}(T_j) = V_F(1.25 \cdot I_{sc}, T_j) \cdot I_{sc} \cdot 1.25$$

To meet the test requirements ($T_j < T_j max$) the following conditions apply:

$$P_{cond}(T_j) < P_{thermal}(T_j)$$

$$P_{cond}(T_j max) = \frac{(T_j max - 75\ °C)}{R_{th(j-a)}}$$

then the maximum forward voltage is

Equation 18

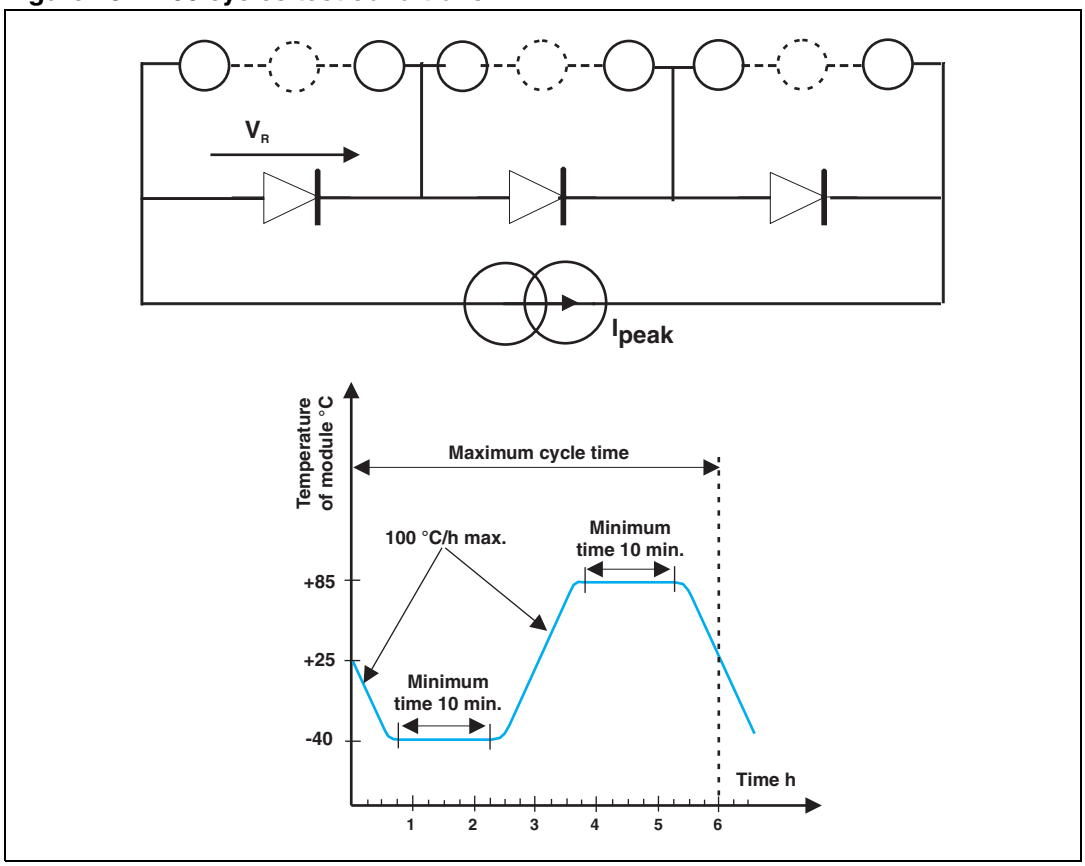
$$V_F max(1.25 \cdot I_{sc}, T_j max) < \frac{(T_j max - 75\ °C)}{R_{th(j-a)}} \cdot \frac{1}{1.25 \cdot I_{sc}}$$

3.2.2 200 cycles

This test is requested for the crystalline silicon terrestrial photovoltaic modules design qualification. It is described in the standard EN61215 paragraph 10.11.

The bypass diode is polarized in reverse when the module temperature is above 25 °C. *Figure 15* illustrates the test conditions.

Figure 15. 200 cycles test conditions



As the diode is in reverse, the junction temperature is very close to the ambient temperature due to low reverse losses. So there is no risk to exceed maximum junction temperature. The critical parameter in this test is the value of voltage when T_{amb} = 25 °C. Actually, the reverse voltage of a diode decreases with the temperature and then the diode V_{RRM} (25 °C) is the higher value and needs to meet the following requirement:

$V_{RRM}(25\ °C) > V_R(25\ °C)$

For an ST Schottky diode, the V_{RRM} is guaranteed at 25 °C.

4 Optimized bypass diode for a given solar panel or junction box

This section describes a method to choose the optimized bypass diode through an application example with a 400 W photovoltaic panel. Its short circuit current (I_{sc}) is 6.4 A and a its total open circuit voltage (V_{oc}) is 85.3 V in STC conditions. This solar panel needs 3 bypass diodes placed in a junction box having $R_{th(j-a)}$ = 30 °C/W.

Step 1: Determine V_{RRM} minimum value

The highest open circuit voltage value for the solar panel (V_{oc}) is for the -40 °C ambient temperature, that is V_{oc} (-40 °C) = 107 V, with a deviation tolerance of 20% applied. Then the maximum reverse voltage applied to each bypass diode is 43 V.

So the V_{RRM} minimum value is 43 V @ -40 °C. In the product range the nearest V_{RRM} value is 45 V.

Step 2: Diode characteristics versus application constraints

The bypass diode must be compatible with the thermal test. In general its maximum junction temperature is 175 °C.

Then the thermal losses can be calculated as:

$$P_{Thermal}(175\ °C) = \frac{(175\ °C - 75\ °C)}{30}$$

$$P_{Thermal}(175\ °C) = 3.33\ W$$

The junction box is able to dissipate 3.33 W when the junction temperature of the diode is 175 °C.

To meet the test requirements ($T_j < T_j max$) the following condition applies:

$$P_{cond}(T_j max) < P_{thermal}\ (T_j max)$$

With this condition the maximum forward voltage at $T_j max$ and $1.25 \cdot I_{sc}$ can be calculated using *Equation 18*:

$$V_F max(1.25 \cdot I_{sc}, 175\ °C) < \frac{(175 - 75)}{30} \cdot \frac{1}{1.25 \cdot 6.4}$$

$$V_F max(8\ A, 175\ °C) <\ 0.417\ V$$

The STPS3045CG is compliant with the thermal test requirements since its $V_F max$ (8 A, 175 °C) = 0.31 V

The forward voltage (V_F) of a Schottky diode is temperature dependent. V_F decreases linearly with temperature and can be calculated using the following:

$$V_F max(8\ A, 175\ °C) = \alpha_{V_F}(175 - 125\ °C) + V_F(8\ A, 125\ °C)$$

$$\text{with } \alpha_{V_F} = \frac{V_F max(8\ A, 125\ °C) - V_F max(8\ A, 125\ °C)}{125 - 25}$$

$$\alpha_{V_F} = -1.8\ mV/°C$$

Then:

$V_F max$ (8 A, 175 °C) = -0.09 + 0.4 = 0.310 V:

Step 3: Eliminate the risk of thermal runaway

As explained in the previous section, the most critical step is the thermal runaway risk that occurs at the diode switching off. In the worst case, the diode will conduct a current very close to I_{sc} = 6.4 A and will switch off with a reverse bias voltage equal to V_{oc} (85 °C)/ 3 = 64.83 / 3 = 21.61 V.

The power conduction losses calculation gives:

$$P_{cond}(T_j) = V_F(I_{sc}, T_j) \cdot I_{sc}$$

With:

$$V_F(I_{sc}, T_j) = V_{T0}(T_j) + R_d(T_j) \cdot I_{sc}$$

$$V_{T0}(T_j) = 0.51 - 2.3 \times 10^{-3} \cdot (T_j - 25)$$

$$R_d(T_j) = 0.2 + 1 \times 10^{-4} \cdot (T_j - 25)$$

The power reverse losses are given by the following equation:

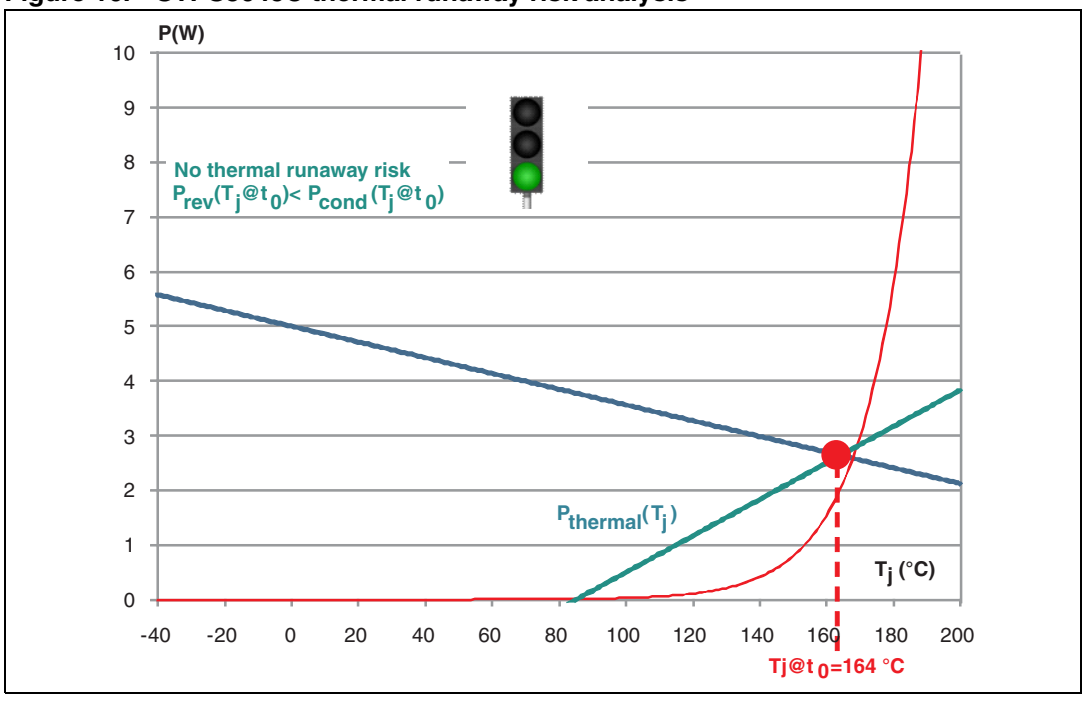
$$P_{rev}(T_j) = 1.51 \cdot 10^{-1} \cdot e^{0.06(Tj-125)}$$

Then we apply the thermal law in order to find the junction temperature at switching time.

$$P_{Thermal}(T_j) = \frac{(T_j - 85\ °C)}{30}$$

Thermal law and power conduction losses curves cross gives the junction temperature at switching time in *Figure 16*.

Figure 16. STPS3045C thermal runaway risk analysis



The junction temperature at switching off is 164 °C. At this junction temperature, the reverse losses are below the conduction losses. In conclusion, there is no risk of thermal runaway with STPS3045CGC.

5 Conclusion

This application note provides the means to select the best bypass diode device based on junction box or PV module specifications. This diode selection will depend on its technology trade off - forward drop voltage versus reverse current. ST offers a broad range of Schottky diode from 10 to 60 A and 20 V to 45 V ratings. Their low leakage current is a distinctive performance that has allowed more than 50 million pieces to be assembled successfully in 2011. Future trends should allow the extension of their maximum temperature to 200 °C while covering the increased maximum current up to 15 A for the stringent junction box thermal test.

6 Revision history

Table 1. Document revision history

Date	Revision	Changes
06-Sep-2011	1	Initial release.