# LM555 and LM556 Timer Circuits

This page presents general information and tips for using the LM555 timer and devices with other letter prefixes. There will be minor internal circuitry differences between 555 timer IC's from the various manufacturers but they all should be useable for the circuits on this page.

If you would like to use any of these ideas, take the time to do some testing before using the LM555 timer in an actual circuit. All of the solutions on this page can also be applied to the LM556 - Dual timer.

Some of the circuits on this page were developed just to see if they would work and have no intended use.

The menu below links to various sections of this page that relate to the items in the index. New additions appear at the bottom of the list.

## - Page Sections -

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## - Other Related Pages -



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## CMOS Versions Of The 555 Timer

All of the information on this page can be applied to the low current, CMOS versions of the 555 timer as well.

However, the CMOS versions have a lower output current rating and may not be able to drive some loads. Also, the outputs of some CMOS timers can source more current than they can sink.

For single sided loads, an NPN or PNP driver transistor can be added to the output of the timer to increase the current capacity of the timer. ( See section 31 of this page for more information. )

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## This Page Is Not Applicable To The LM558

This page does not apply the LM558 - Quad Timer IC which is significantly different when compared to the 555 and 556 timers.

The differences include: (1) The output of each 558 timer is an open collector transistor with a 100 milliamp current capacity while the 555 and 556 timers have bipolar outputs with a 200 milliamp capacity. (2) The TRIGGER input of the 558 is EDGE Triggered while the TRIGGER input of the 555 and 556 timers are LEVEL Triggered.

Individual LM558 timers are not designed to operate in an astable mode. Two 558 timers must be connected in a loop to make an astable oscillator.

- EDGE Triggered - means that the change in the output state of the timer is caused by a quickly falling or rising voltage at the input terminal. If the input voltage changes too slowly the output will not switch states.

- LEVEL Triggered - means that the change in the output state of the timer is caused when the voltage at an input terminal falls bellow or rises above a preset level. The rate at which the voltage changes is not important.

The THRESHOLD input terminals for the 555, 556 and 558 timers are all LEVEL triggered.

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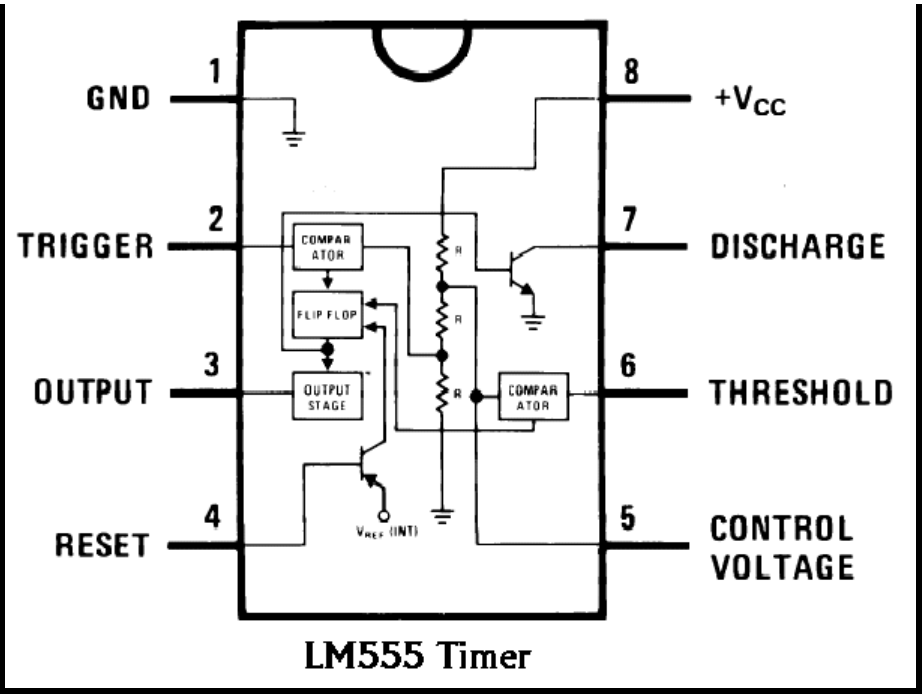
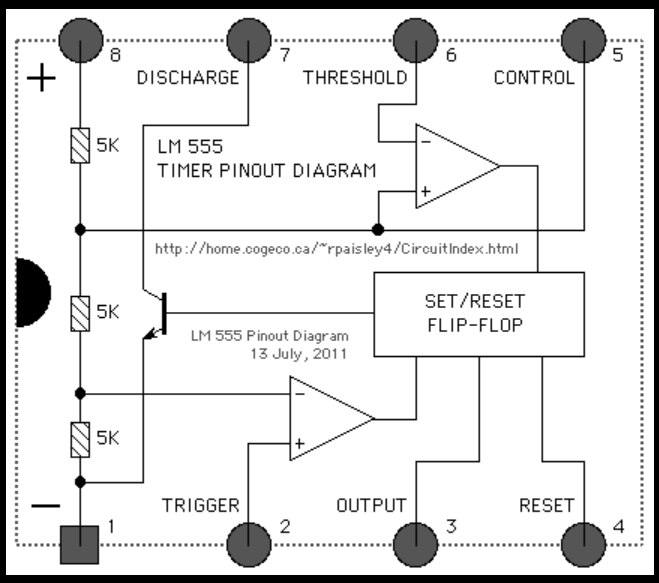
**LM555 Timer Internal Circuit Block Diagram**

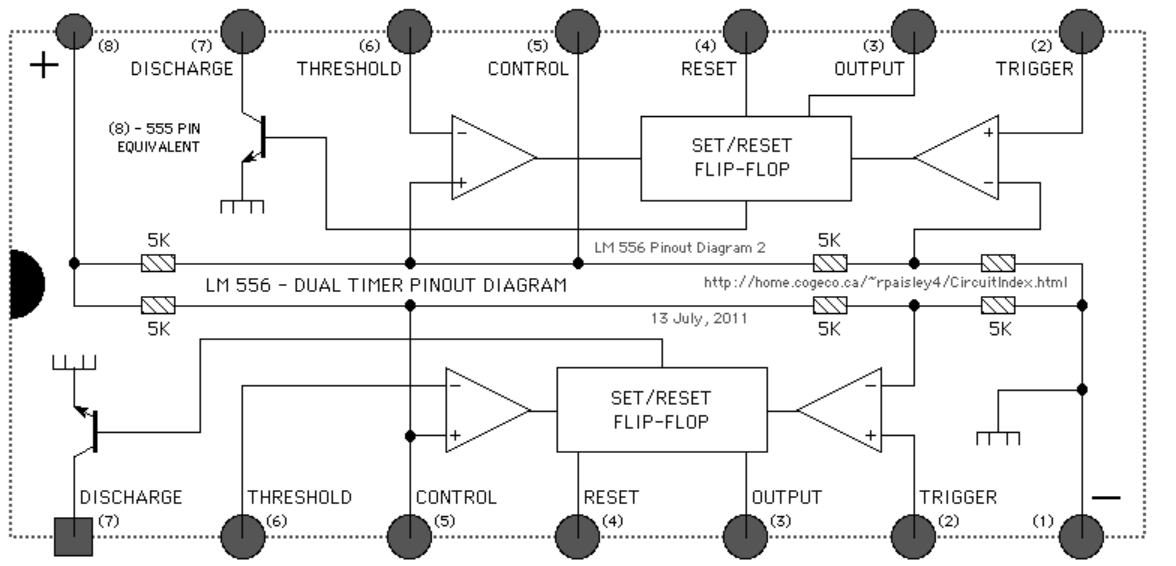



**LM555 Timer Internal Circuit Block Diagram**




Print the diagram in the centre of a sheet of paper and then draw a circuit using the ICs pin locations.

**LM556 Timer Internal Circuit Block Diagram**




Print the diagram in the centre of a sheet of paper and then draw a circuit using the ICs pin locations.

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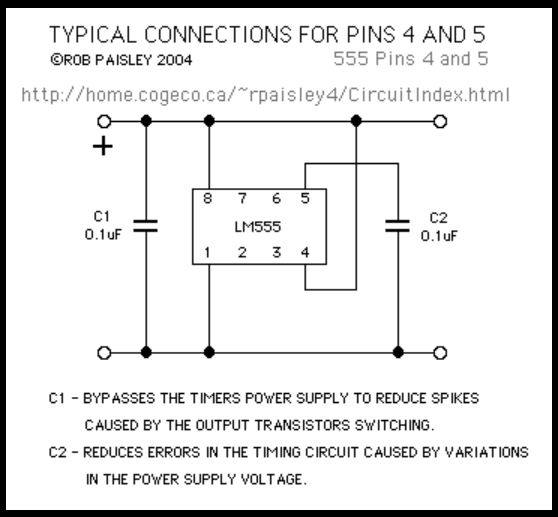
## RESET And CONTROL Terminal Notes

Most of the circuits at this web site that use the LM555 and LM556 timer chips do not show connections for the **RESET** and **CONTROL** inputs. This was done in order to keep the schematics as simple as possible.

If the **RESET** terminal of a 555 or 556 timer is not going to be used, it is normal practice to connect this input to the supply voltage. If the **RESET** terminal is left unconnected the operation of the timer will not be affected, however, the **RESET** of CMOS version of these timers should not be left unconnected as the inputs of these devices are more sensitive and this may cause problems.

In many cases the **CONTROL** input does not require a bypass capacitor if a well regulated power supply is used. However, it is good practice to place a 0.1 microfarad (C2) capacitor at this terminal to minimize voltage spikes during transitions of the timer's output transistors.

It is also good practice to place a 0.1uF bypass capacitor (C1) across the power supply and located as close to the IC as possible. This will also reduce voltage spikes when the output transistors of the timer change states.




**Typical Pin 4 And 5 Connections**

Note - If the period of the power supply variations is short when compared to the period of the timer, the overall effect of C2 is reduced.

For example; If the power supply - ripple voltage is 120 Hz and the oscillator frequency is 1000 Hz then C2 will have greater benefit than if the oscillator frequency is 10 Hz.

Therefore, at low astable frequencies or long monostable times the effectiveness of a capacitor at the CONTROL input is less than at higher frequencies and short pulse times.

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## Calculation Value Notes

Data sheets for the 555 Timer use the value 1.44 and 0.693 as constants in the timing calculations depending on the way in which the equation was written. While these numbers are not exact reciprocals of one another they are close enough to be used without concern.

For ease of use, the calculators on this page have capacitor values entered in microfarads. This value is multiplied by the calculator to produce the correct result. (1uF = 0.000,001F = 1 X $10^{-6}$F)

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# TIMING CALCULATORS FOR THE LM555

With Schematic diagrams

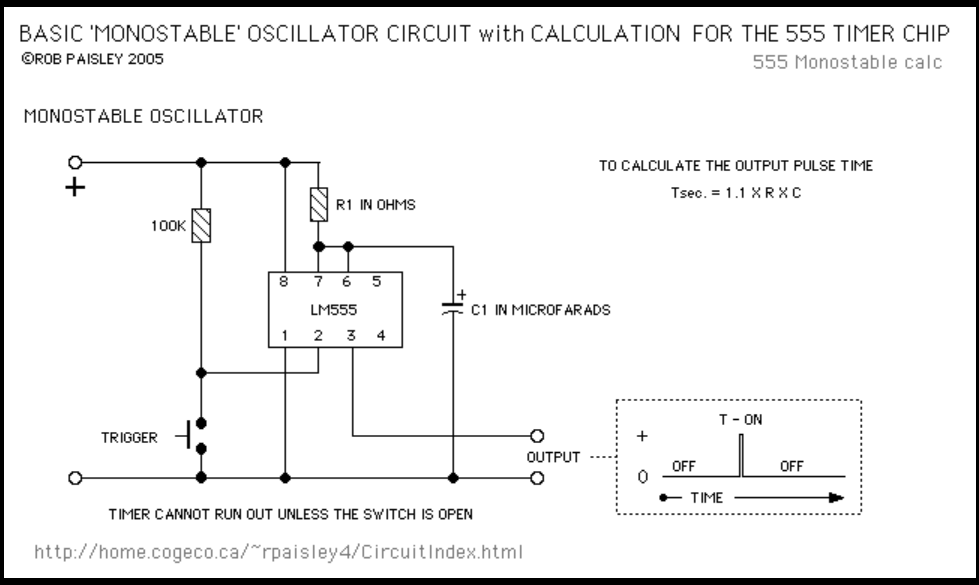
**LM555 - MONOSTABLE OSCILLATOR CALCULATOR**

| Value Of R1 | Value Of C1 | | Output Pulse |
|---|---|---|---|
| **Ohms** | **Microfarads** | Calculate | **Seconds** |

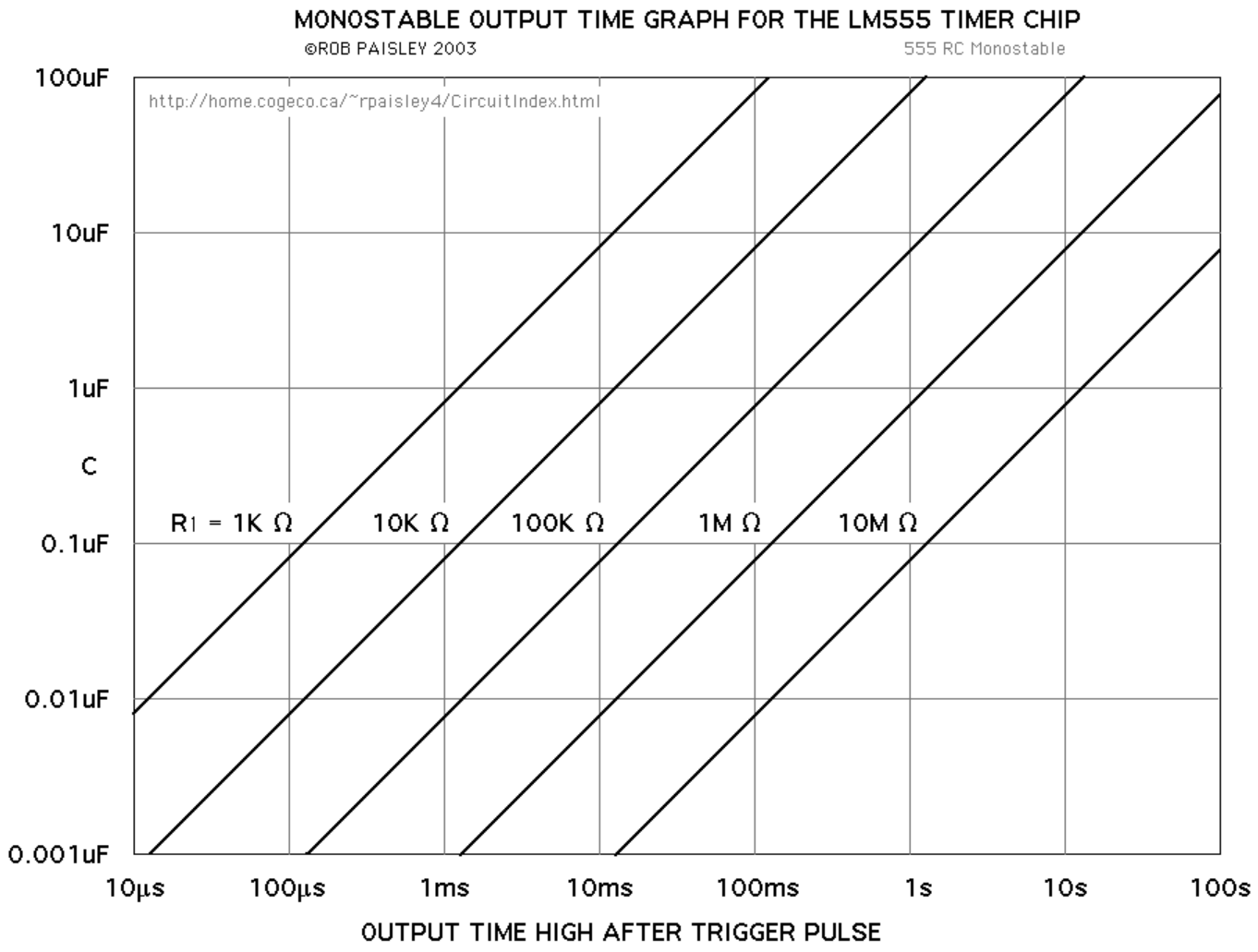
**Resistor values are in Ohms (1K = 1000) - Capacitor values are in Microfarads (1uF = 1)**

**NOTE:** The leakage currents of electrolytic capacitors will affect the actual output results of the timers. To compensate for leakage it is often better to use a higher value capacitor and lower value resistors in the timer circuits.

**LM555 Monostable Oscillator Circuit Diagram**




**LM555 Monostable Oscillator Output Time Chart**




RESET And CONTROL Input Terminal Notes

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**LM555 - ASTABLE OSCILLATOR CALCULATOR**

Value Of R1 **Ohms**

Value Of R2 **Ohms**

Value Of C1 **Microfarads**

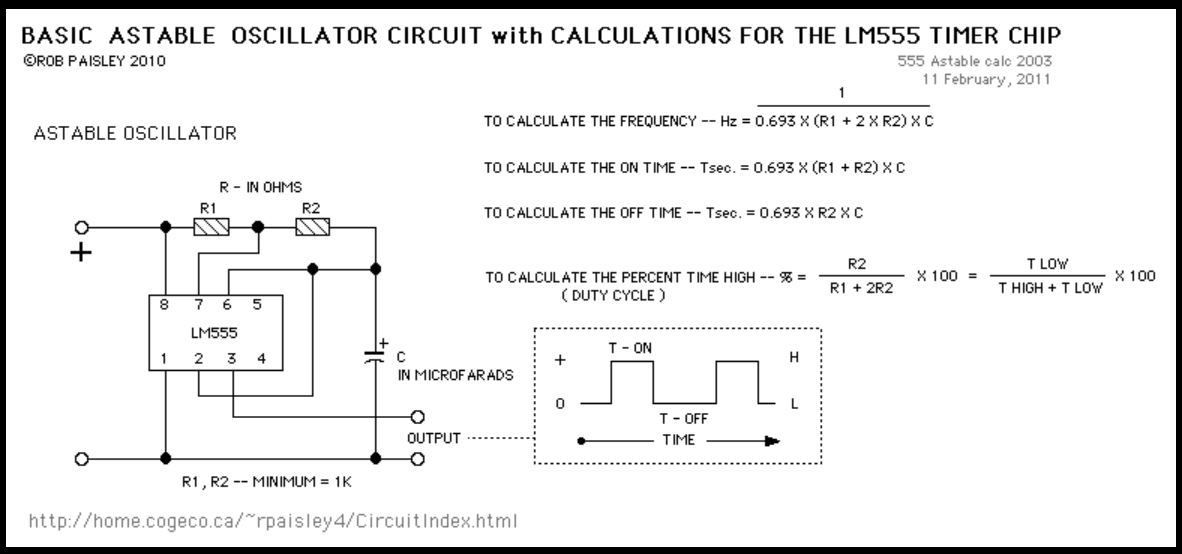
Calculate

| Output Time HIGH | Output Time LOW | Output Period HIGH + LOW | Output Frequency | Output Duty Cycle |
|---|---|---|---|---|
| **SECONDS** | **SECONDS** | **SECONDS** | **HERTZ** | **PERCENT** |

**Resistor values are in Ohms (1K = 1000) - Capacitor values are in Microfarads (1uF = 1)**

**NOTE:** The leakage currents of electrolytic capacitors will affect the actual output results of the timers. To compensate for leakage it is often better to use a higher value capacitor and lower value resistors in the timer circuits.

**LM555 Astable Oscillator Circuit Diagram**

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The next calculator can find the capacitance needed for a particular output frequency if the values of R1 and R2 are known.

**LM555 - ASTABLE CAPACITOR CALCULATOR**

Value Of R1

**Ohms**

Value Of R2

**Ohms**

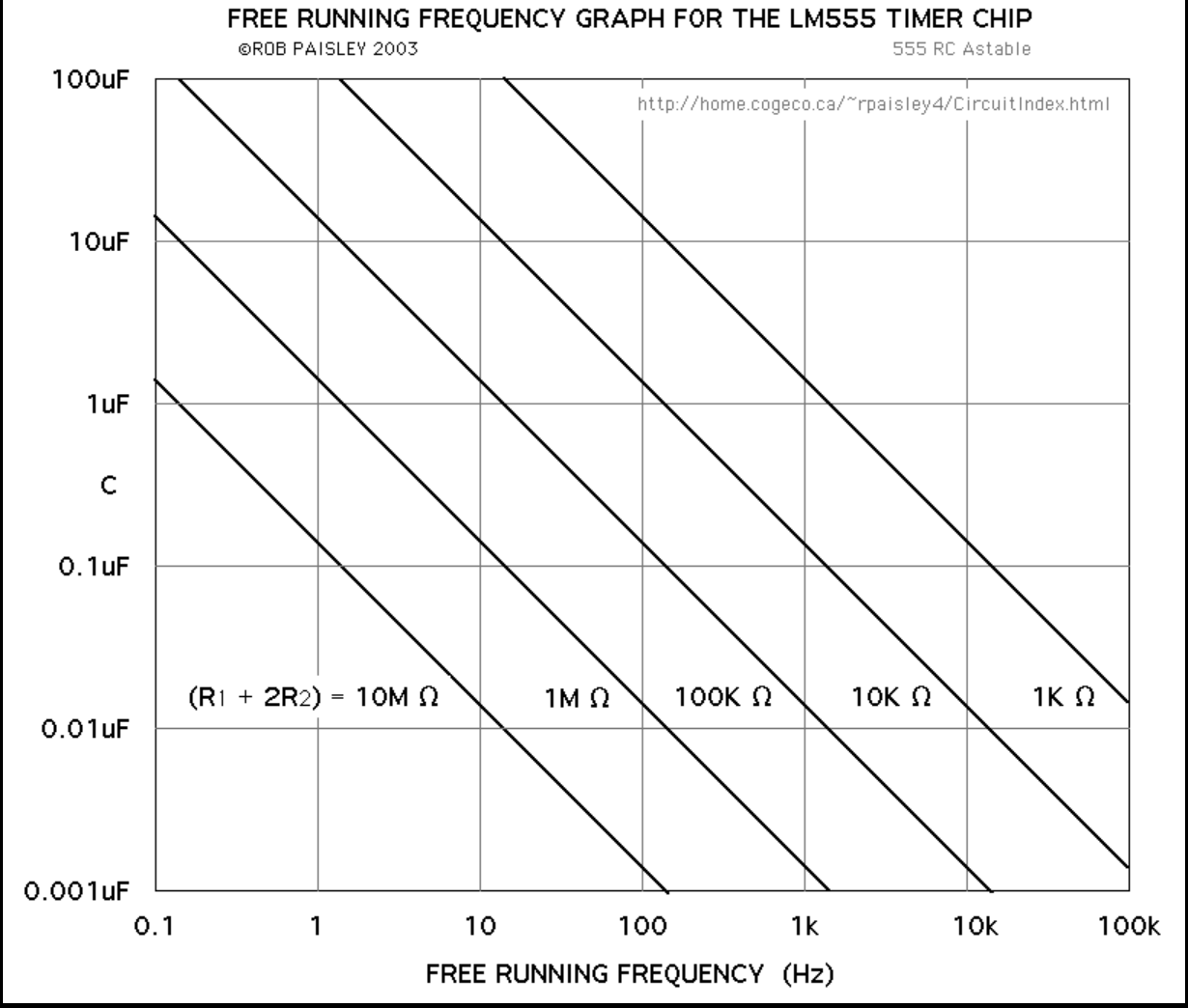
Frequency Desired

**Hertz**

Calculate

Capacitance uF

**LM555 Astable Oscillator - Free Running Frequency Chart**

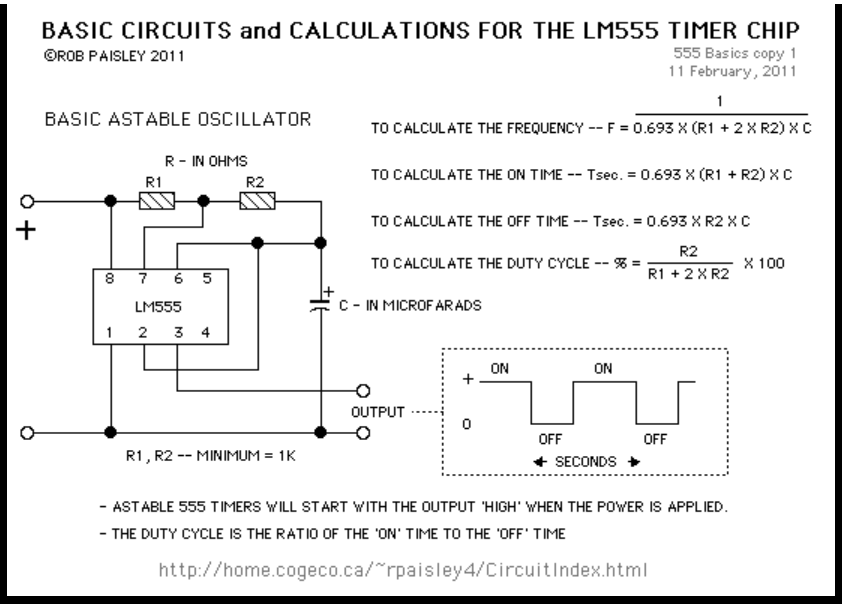



RESET And CONTROL Input Terminal Notes

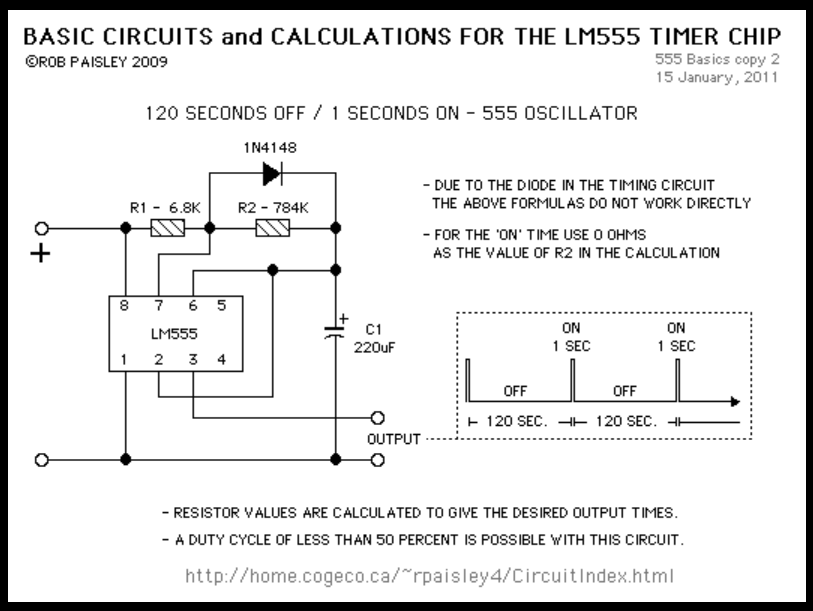
## Basic Circuits For The LM555 Timer

The following diagrams show some basic circuits and calculations for the LM555 timer.

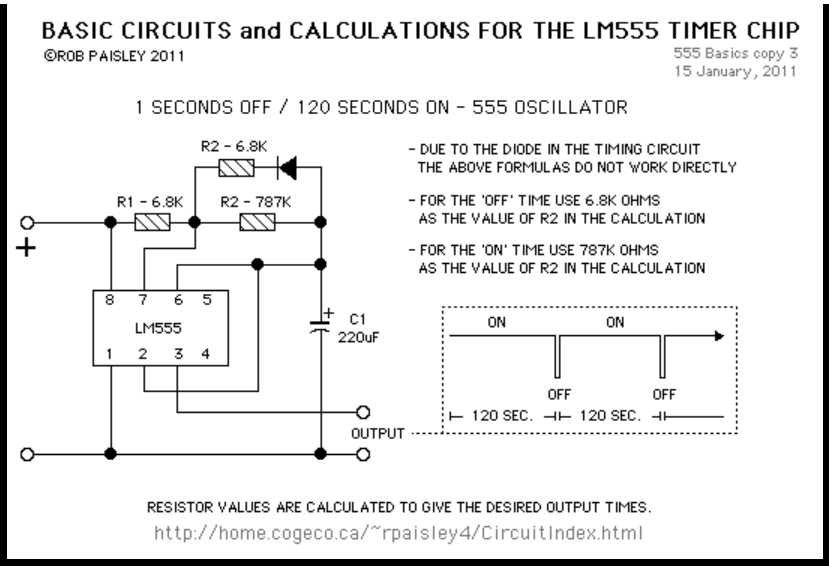
**Circuit 1**



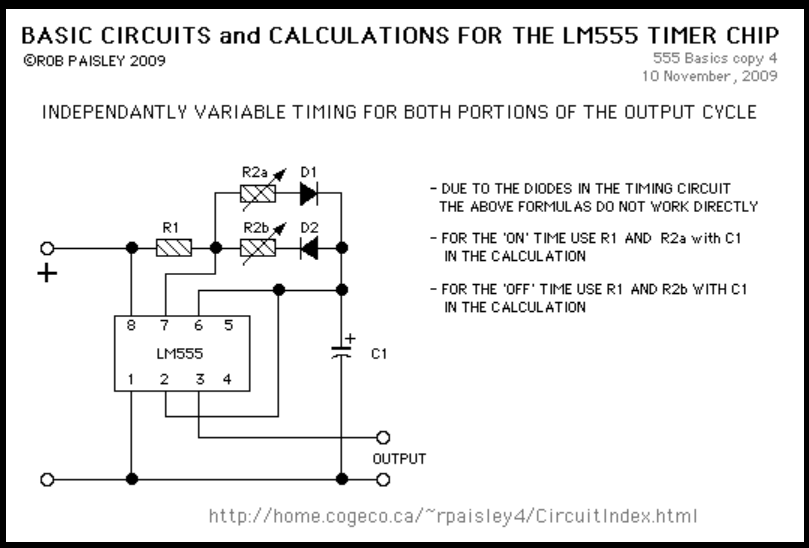

**Circuit 2**



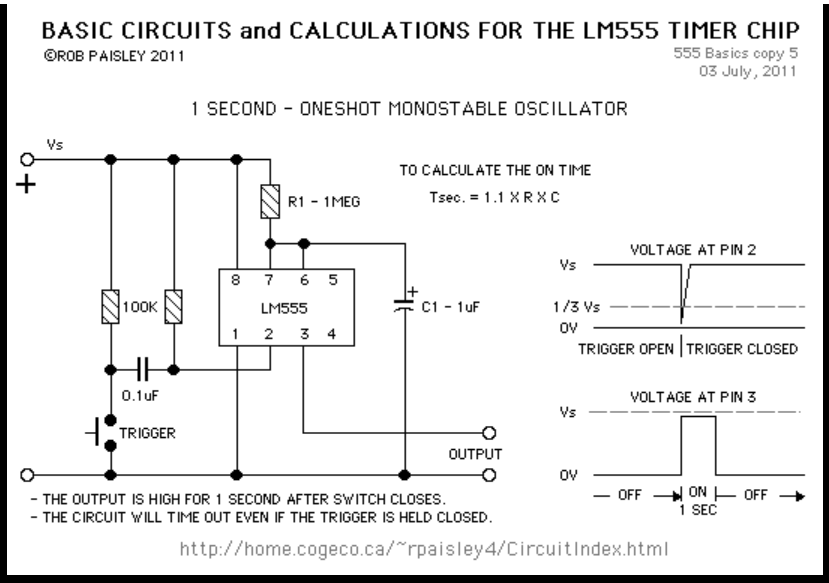

**Circuit 3**




**Circuit 4**




**Circuit 5**




Circuit 5 also has a trigger input that can remain closed and still allow the timer to complete its cycle. This means that the trigger input pulse can be longer than the output pulse.

RESET And CONTROL Input Terminal Notes

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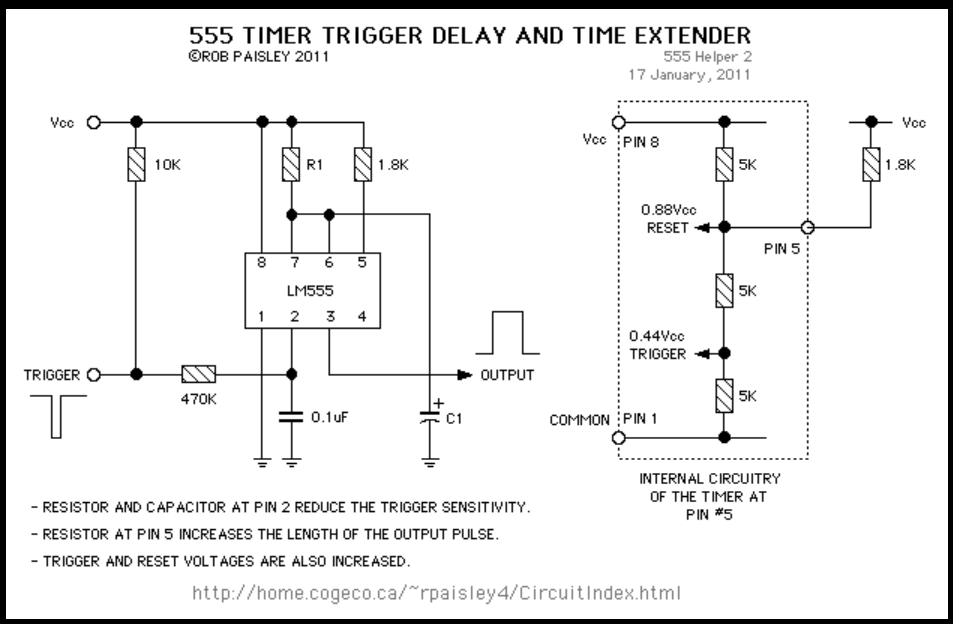
## Triggering And Timing Helpers For Monostable Timers

The LM555 timer and its twin brothers the LM556 are cornerstones of model railroad electronics but the sensitivity of the trigger input gives rise to many false triggering problems. The addition of a 470K ohm resistor and a 0.1uF capacitor at the TRIGGER input (Pin 2) will provide a delay of approximately 1/20th of a second from the time the input goes to zero volts until the trigger threshold of 1/3Vcc is reached. This short delay can eliminate false triggering in most cases and if the problem persists the value of the capacitor or resistor can be increased as needed.

The following schematic shows two additions to the basic 555 timer circuit. One reduces the trigger sensitivity and the other will double the output pulse duration without increasing the values of R1 and C1.




**555 Timer Helpers Schematic**

The addition of a resistor and capacitor to the trigger will not work for very short output pulses as there is also a short delay in

the recovery of the trigger terminal voltage.

The second addition is a helper that will extend the timers output duration without having to use large values of R1 and/or C1. Connecting a 1.8K ohm resistor between the supply voltage and pin 5 of the 555 timer chip the output pulse duration will be approximately doubled.

The boxed in area of the drawing shows the internal circuit at pin 5 of the timer with the 1.8K resistor added. The voltage at pin 5 will be increased from 0.66Vcc to 0.88Vcc which is approximately equal to the voltage across the capacitor after two time constants*. This allows the same output time to be achieved with a smaller resistance or capacitance value thus reducing the error caused by the capacitor leakage current. Conversely, for a given value of R1 and C1, the output time will be doubled by the addition of the resistor at Pin 5.

* - One time constant is equal to R (Ohms) times C (Farads) in seconds. In terms of voltage, one time constant is equal to a rise in voltage across the capacitor from 0 to 63.2 percent its maximum voltage. (1uF = 0.000,001F = 1 X $10^{-6}$F)

The trigger and reset voltage levels of the timer will also be increased with the addition of the resistor to pin 5 but this should have no effect in most applications.

To achieve long output times, electrolytic capacitors are often used for C1 and the value of R1 can be as high as 1 Megohm. However with high resistance values for R1 the leakage current of the timing capacitor (C1) becomes a significant factor in the operation of the timer.

The circuit will run much longer than expected and may never time out if the leakage current is equal to the current through the resistor at some voltage. Tantalum capacitors could be used as they have very low leakage currents but these are expensive and not available in large capacitance values.

Adding a resistor to the CONTROL terminal is not an ideal solution to solving long duration timing situations but should work for pulse times of less than ten minutes.

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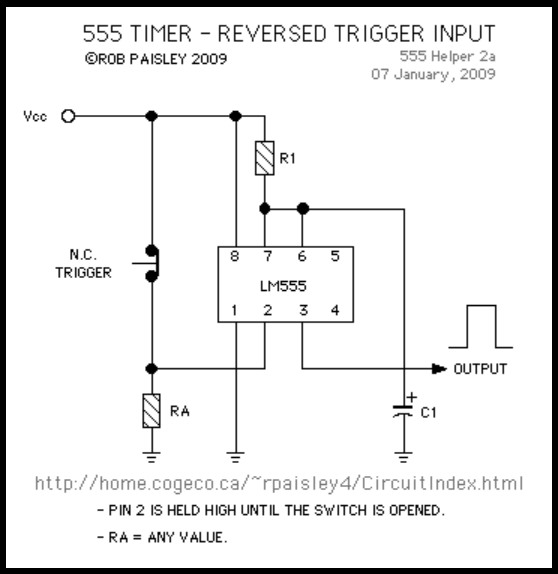
## Reversed Trigger Input Control Of 555 Timers

The following method allows the timer to be triggered by a normally closed switch. This would be useful in applications such as intrusion alarms where the protection circuit is broken if a window or door is opened




**Reversed Trigger Input**

RESET And CONTROL Input Terminal Notes

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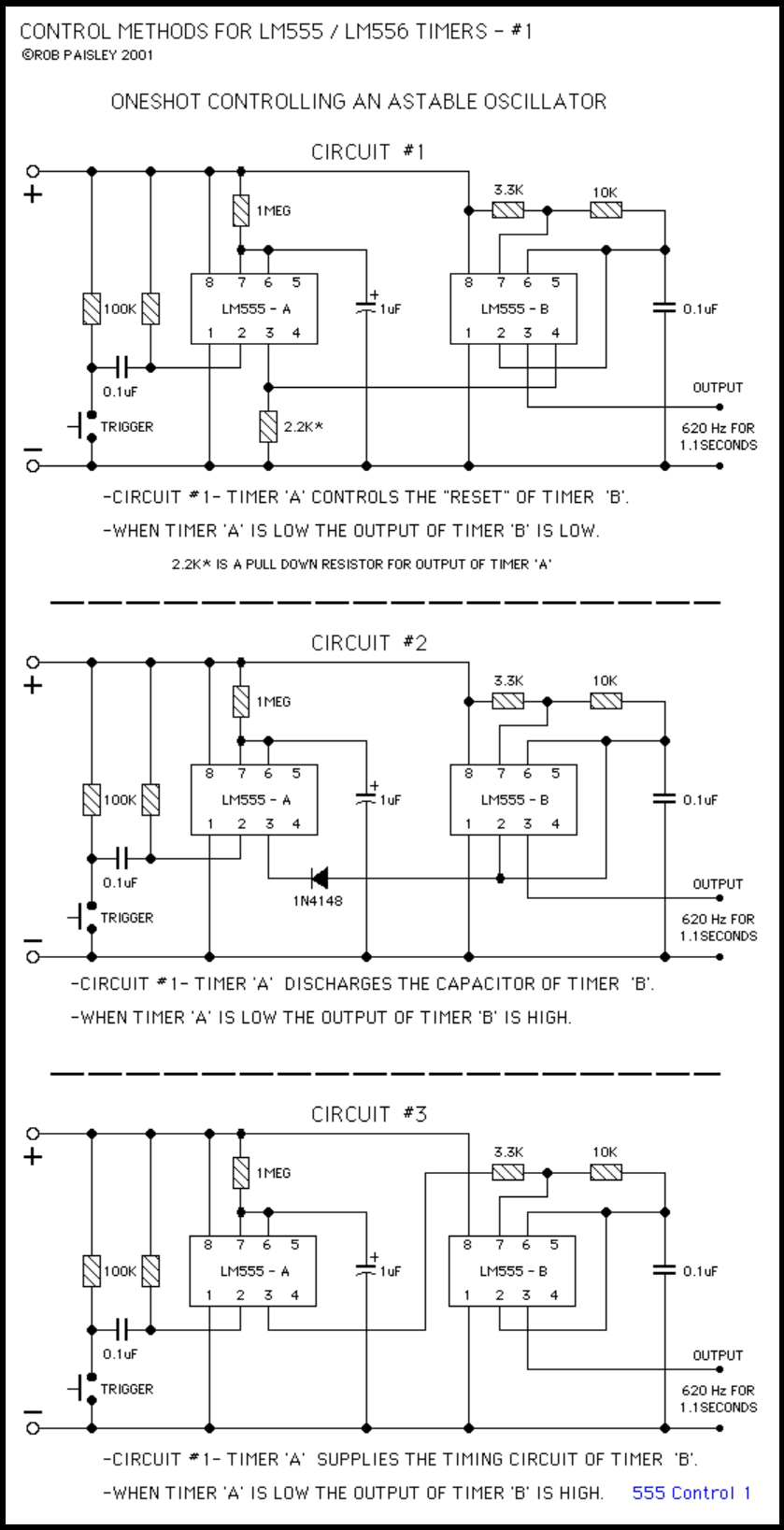
## Controlling Circuits For LM555 Timers

The following diagrams show some methods of using one timer to control a second . Some of these are unusual but still practical and can provide ideas for other control schemes.

In the following diagrams, a ONESHOT oscillator controls an ASTABLE oscillator. Three methods are shown.




**LM555 Control methods #1 schematic**

RESET And CONTROL Input Terminal Notes

## Advanced Circuits For The LM555 Timer

The following diagrams show some advanced circuits for the LM555 timer. These circuits were developed to provide certain functions that are not typically associated with this device.

The parts values in these circuits were selected for testing purposes and can be adjusted to suit the needs of a particular application as long as the normal operating parameters of the LM555 are maintained.

Before using any of these circuits for specific applications they should be tested to determine the best values for the components and the practicality of their use.

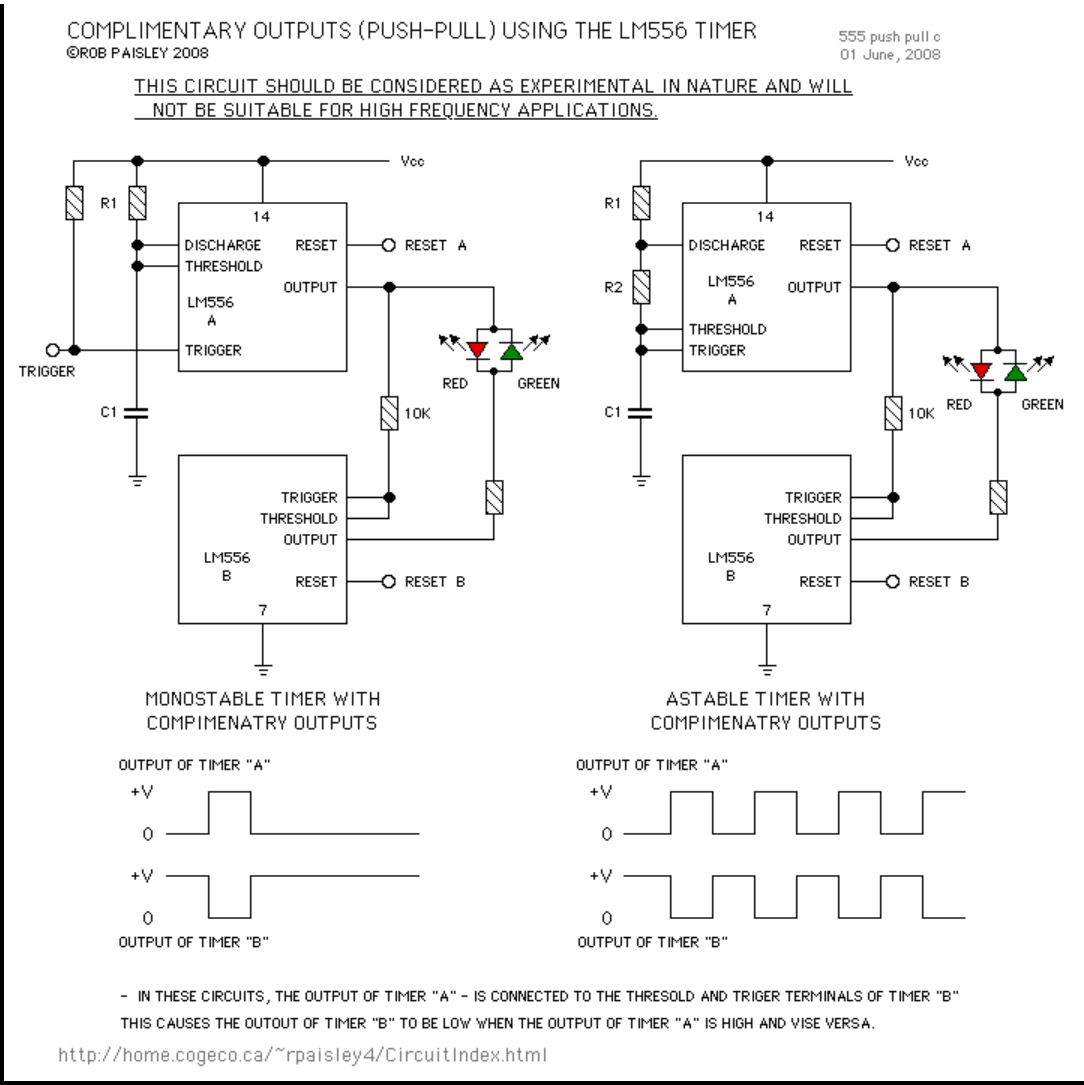
## LM556 Timers with Complimentary or Push-Pull Outputs

In the next circuit an LM556 - dual timer IC is configured so that the output of the second timer is 180 degrees out of phase with the first.

This is done by connecting the OUTPUT of timer A to the TRIGGER and THRESHOLD terminals of timer B. The 10K ohm resistor limits the current that can flow into the THRESHOLD terminal of timer B.

Due to the ability of the timers to source or sink current, the current from one timers output can flow into the other timer's output depending on which output is HIGH or LOW. The typical output conditions that are referenced to ground or supply are also available and in fact all three could be used at the same time.

Circuits for both Astable and Monostable versions of this method are shown on the diagram.




**LM555 Complimentary Outputs schematic**

Timer B in this method acts as a voltage comparator and has no timing function. It is a slave to timer A.

Normal triggering methods and period lengths are not affected.

Both timer's RESET terminals are available and can be used individually or together.

Due to the unusual nature of this type of circuit testing should be done to determine if it is suitable for the use intended. The circuit is usable at frequencies below 1000 Hz.

RESET And CONTROL Input Terminal Notes

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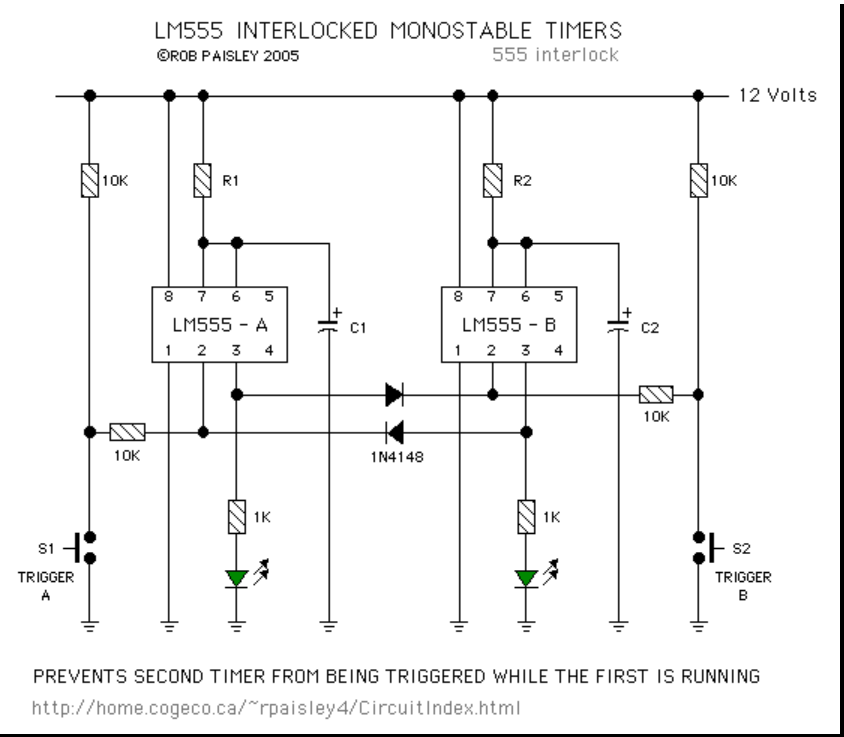
## Interlocked Monostable Timers

In the following circuit the timers are interlocked so that while one timer is running the second timer cannot be triggered.

This is done by connecting the OUTPUT of each timer to the TRIGGER of the other through a diode and placing a resistor in the trigger circuit. The resistor limits the current from the opposite timers output when the trigger is closed on the stopped timer.




**LM555 Interlocked Timers schematic**

Normal triggering and timing lengths are not affected by this method.

RESET And CONTROL Input Terminal Notes

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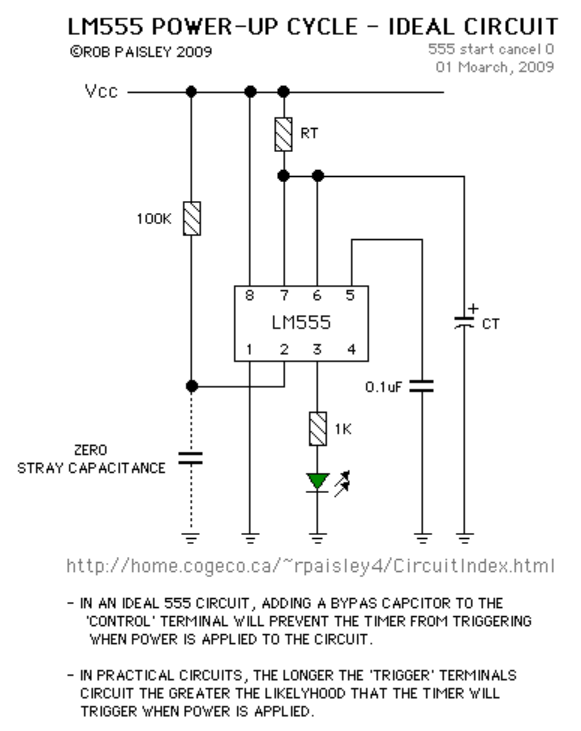
# Power-Up Reset For 555 Timers

Typical monostable 555 timer circuits will automatically trigger and start a timing cycle when power is applied to the circuit. Stray or installed capacitance at the TRIGGER terminal of the timer is largely responsible for this triggering but it is also caused by the nature of the 555 timer's internal circuitry as well.

Stray capacitance can be from a number of sources but a typical cause is the wires that connect a push button used to start the timer.

In an ideal circuit, where there is no stray capacitance at the TRIGGER input, a small capacitor at the CONTROL terminal could prevent the timer from triggering .




**LM555 Power-Up - Ideal Circuit Conditions**

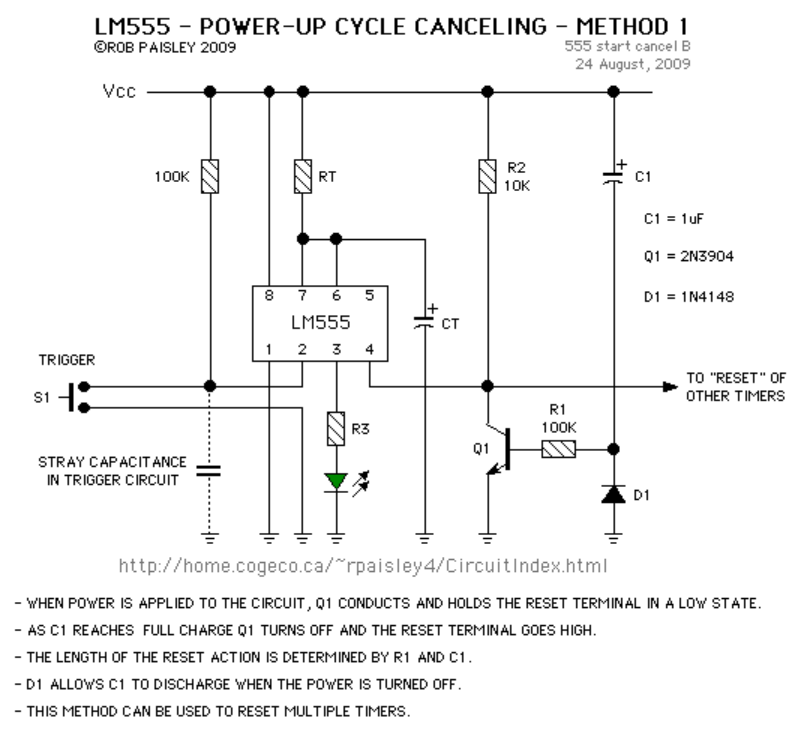
## Practical Circuit Conditions

If there is stray or installed capacitance at the TRIGGER terminal, when the power is applied to an LM555 circuit the timer will immediately be triggered and start a cycle. This can be a undesirable if the period is long and there is no way to stop the cycle.

To prevent timer from starting, a simple RC timing circuit can be added to the timer's RESET terminal so that when power is applied to the circuit, the timer is automatically held RESET by transistor Q1 until C1 is almost fully charged.

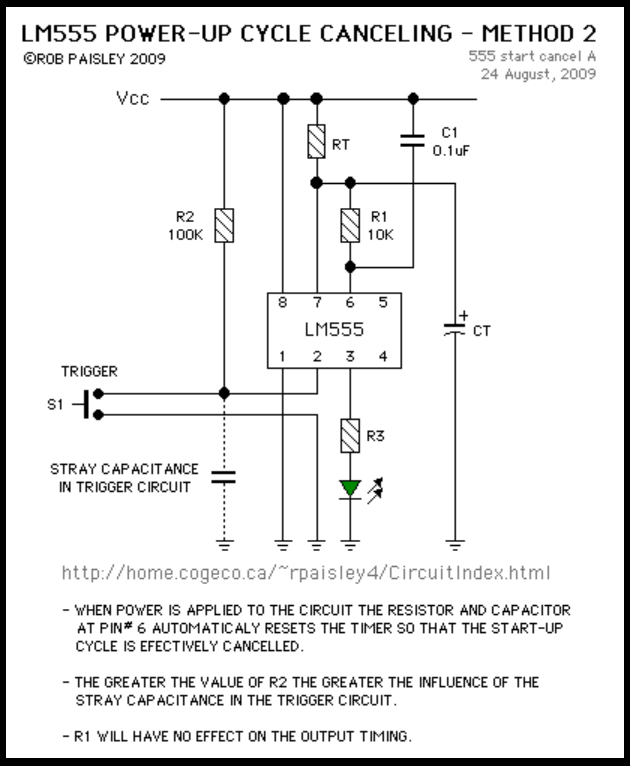
The length of the resetting action can roughly be determined by R1 X C1 X 3 .

The example circuit shows a monostable oscillator but the method could also hold an astable 555 oscillator in a reset condition at power-up.




**LM555 Power-Up Reset Method 1**

The following circuit is another method of stopping the timing cycle at power-up. In this case, a pulse is sent to the THRESHOLD terminal which stops the timing cycle when the power is applied.




**LM555 Power-Up Reset Method 2**

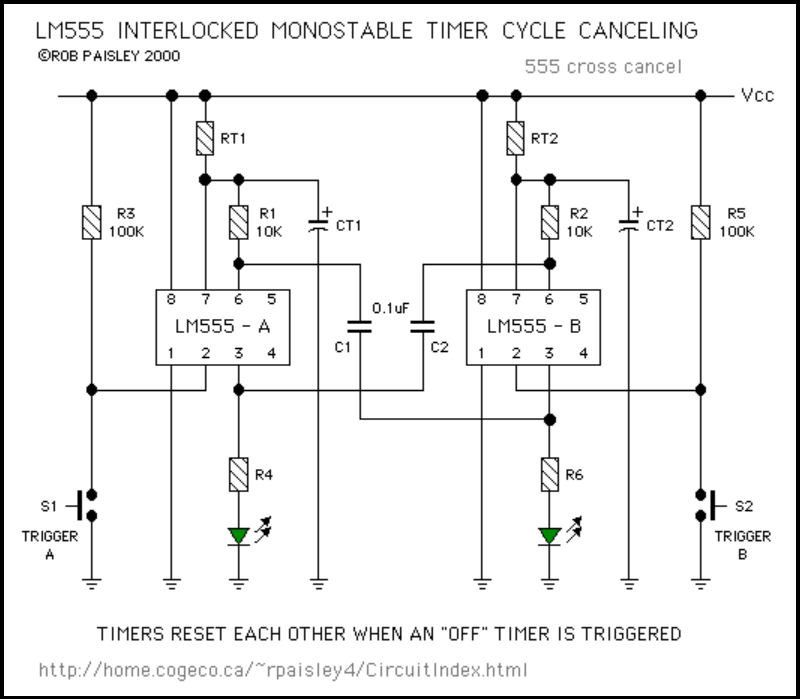
RESET And CONTROL Input Terminal Notes

## Cross Canceling For Monostable Timers

The following diagram shows a method that allows one LM555 timer to RESET another timer so that, for example, if timer 'A' is running; When timer B is triggered, timer A will be reset.

This means that only one timer can be running at a time.

As with the 'Power-Up Reset For Monostable Timers' circuit above, when the power is applied to the circuit both timers are RESET.




**LM555 Cross Canceling Timers schematic**

Normal triggering and timing lengths should not be affected by this method.

The trigger switch of the running timer must be OPEN for the RESET to occur.

RESET And CONTROL Input Terminal Notes

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## RS Flip-Flop Made With A LM556 Timer

The next circuit is for a hybrid - SET / RESET type of logic Flip-Flop that is constructed from an LM556 - Dual Timer.

The design is crude but effective for very low speed applications. Its greatest asset is that the outputs of the LM556 are capable of driving current loads of up to 200 milliamps with a minimal voltage loss.

This circuit was originally developed to drive "Stall Motor" type switch machines that are used on model railroads. These motors use low voltage DC and draw approximately 15 milliamps when they are in a stalled condition.

Due to the design of the LM556 timer chip there are multiple output options available in this circuit. These include the normal timer outputs which are bipolar and the DISCHARGE terminals, (PINS 1 and 13), that are open collector circuits.

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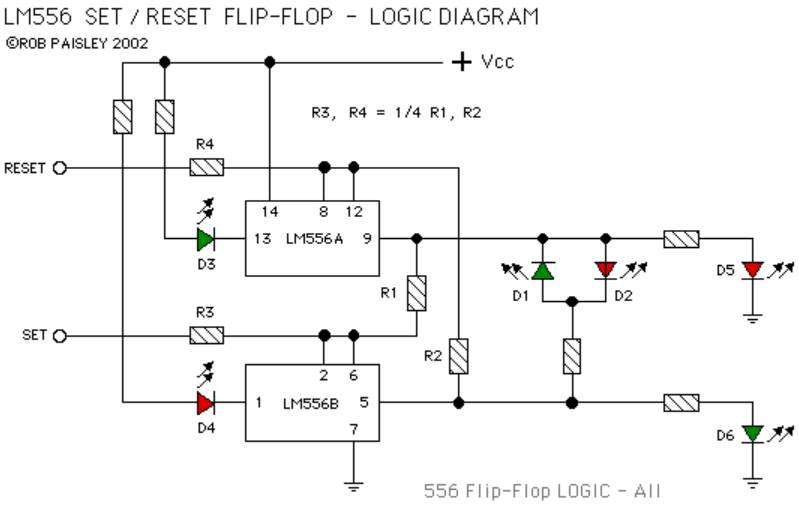
## LM556 Flip-Flop Truth Table

The following diagram is for a test version of the LM556 Flip-Flop circuit used to create a "Truth Table" that shows the OUTPUT states for a given INPUT state.




TRUTH TABLE FOR THE LM556 FLIP-FLOP CIRCUIT ABOVE

| | INPUT | | PIN | | LED | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| STATE | SET | RESET | 9 | 5 | D1 | D2 | D3 | D4 | D5 | D6 |
| 1 | LOW | HIGH | LOW | HIGH | ON | OFF | ON | OFF | OFF | ON |
| 2 | HIGH | LOW | HIGH | LOW | OFF | ON | OFF | ON | ON | OFF |
| 3 | LOW | LOW | HIGH | HIGH | OFF | OFF | OFF | OFF | ON | ON |
| 4 | HIGH | HIGH | LOW | LOW | OFF | OFF | ON | ON | OFF | OFF |

INPUTS - HIGH = Vcc / LOW = 0 Volts

http://home.cogeco.ca/~rpaisley4/CircuitIndex.html

## Logic Function diagram

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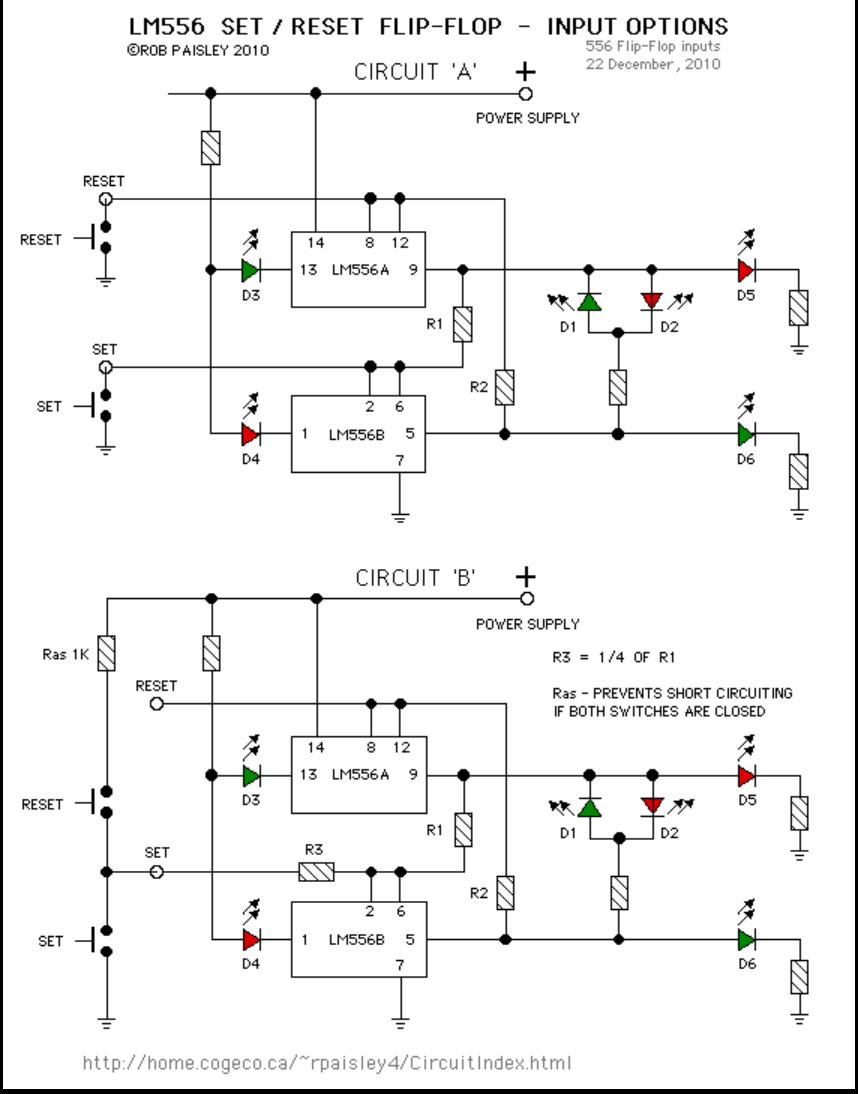
## LM556 Flip-Flop Input Options

The next diagram shows basic input options that can be used with the LM556 Flip-Flop circuit. In actual applications the push buttons could be replaced with or supplemented by electronic input devices.




## Input Options schematic

In circuit A the SET and RESET inputs would be brought to 0 Volts to change the state of the Flip-Flop.

In circuit B the SET input would be switched between 0 Volts and the supply voltage to change the state of the Flip-Flop. The RESET terminal is unconnected.

In both circuit A and B, when the push buttons are OPEN the Flip-Flop will remain in its last state until the opposite signal is applied to an input.

Circuits A and B also show two methods of connecting the LED's at terminals 1 and 13. The input method in circuit B would not be practical to produce the STATE 3 condition shown in the Truth Table on the previous diagram.

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## LM556 Flip-Flop Notes

- **If you would like to make use of this type of circuit, please take the time to build one and do some experimenting to determine if the design will suit your needs.**
- This circuit was developed for low speed operation. It was found however to operate satisfactorily at clock speeds in excess of 10 kHz.

  The values of R1 and R2 in this test were 100K ohms. The value of R3 was 22K ohm.
- As can be seen in the schematics, the OUTPUT of one timer is fed, through a 10K ohm current limiting resistor (R1 and

R2), to the TRIGGER and THRESHOLD inputs of the other. The value of this resistor is not critical and is largely dependent on the impedance of the INPUT devices used to trigger the stage changes.

If resistors R1 and R2 are not used the operation of the circuit becomes unstable.

- Due to the internal circuitry at THRESHOLD terminals (PINs 6 and 12) of the LM556 timers, resistors R3 and R4 are needed to limit the current that can flow into these terminals. The value of resistors R3 and R4 should be approximately 1/4 the value of resistors R1 and R2 so that the proper voltage ratios for changing states can be achieved.

  The R3 resistor is not required if the inputs are not going to be driven to a HIGH state.

- The cross coupling of the timers OUTPUT and TRIGGER/THRESHOLD terminals gives the circuit its FLIP-FLOP action and causes the outputs of the timers to be forced alternately HIGH or LOW. This action only applies to states 1 and 2 in the truth table shown above.

- For this circuit to have a memory function such as that of a SET / RESET type Flip-Flop the input terminals must float when no input signal is present. They cannot be held HIGH or LOW as is the case with TTL devices.

- The maximum current the the outputs of the LM556 timers can source or sink is 200 milliamps.

- These circuits do not need a regulated power supply but the voltage should be well filtered.

- Any of the LED's in the circuit could be replaced by an optoisolator, small relay or low current DC motor.

RESET And CONTROL Input Terminal Notes

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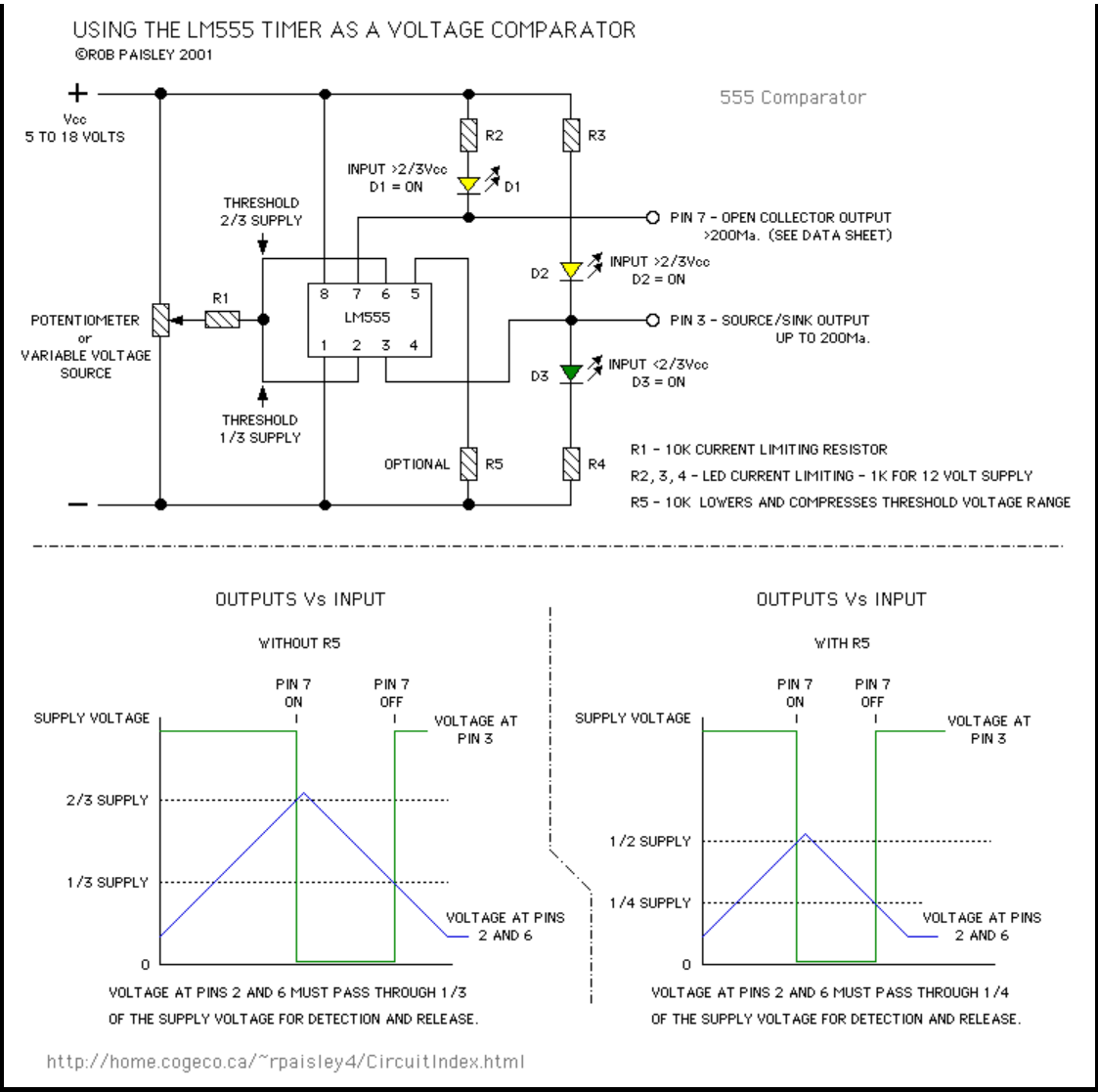
## LM555 Timer Used As A Voltage Comparator Or Schmitt Trigger

The next section shows how an LM555 timer can be used as a voltage comparator or a Scmitt Trigger with a large offset voltage. The 555 timer is not well suited for this application but it is one that is in wide use with model railroaders.

Shown on the schematic is a secondary output that uses the open collector at the DISCHARGE terminal (Pin 7) of the timer. This output can sink up to 200 milliamps and would be ideal for driving relays.

The main disadvantage to using this circuit is the the large dead-band (1/3Vcc) between upper and lower threshold voltages. An optional resistor, R5, can be added to the circuit to lower and compress the detection voltage range but this only partially alleviates the problem.

**LM555 Voltage Comparator / Schmitt Trigger**




The two graphs at the bottom of the diagram show the input voltages at which the OUTPUT of the LM555 will change states. The effect that resistor R5 has on the circuit can be seen in the right hand graph.

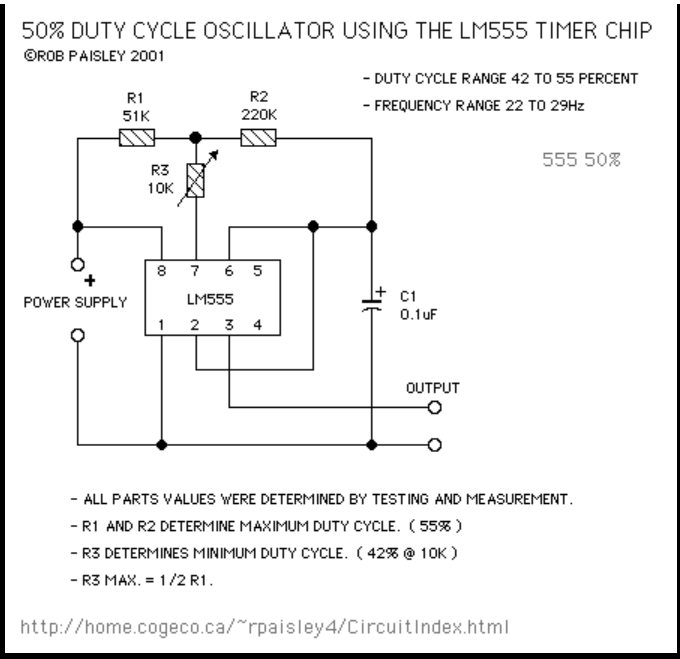
RESET And CONTROL Input Terminal Notes

## 50% Output Duty Cycle (Variable)

The LM555 timer can achieve a 50 percent duty cycle as shown in the next diagram. The duty cycle adjustment range of the give components values is from 42 to 55 percent.

Resistors R1 and R2 were selected first and then resistor R3 was selected to give the best control range based on measurements at the output of the timer.

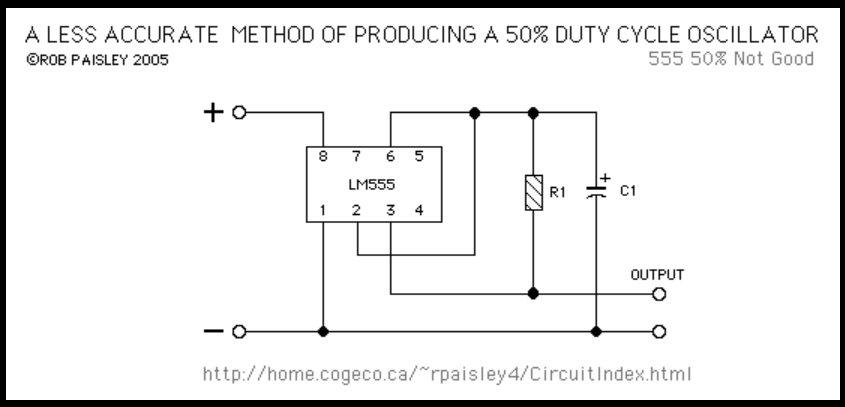
The major disadvantage of using the LM555 in this manner is that the output frequency changes as the duty cycle changes.




**50% Duty Cycle schematic**

## For The Record

The circuit shown in the next diagram is not an accurate method of producing a 50 percent duty cycle using 555 timers, either bipolar or CMOS types. The circuit can produce a duty cycle that is close to 50 percent but when a load is added to the output of the timer, the voltage drops across its output transistors will increase and the duty cycle will shift.




**Not Accurate 50% Duty Cycle schematic**

RESET And CONTROL Input Terminal Notes

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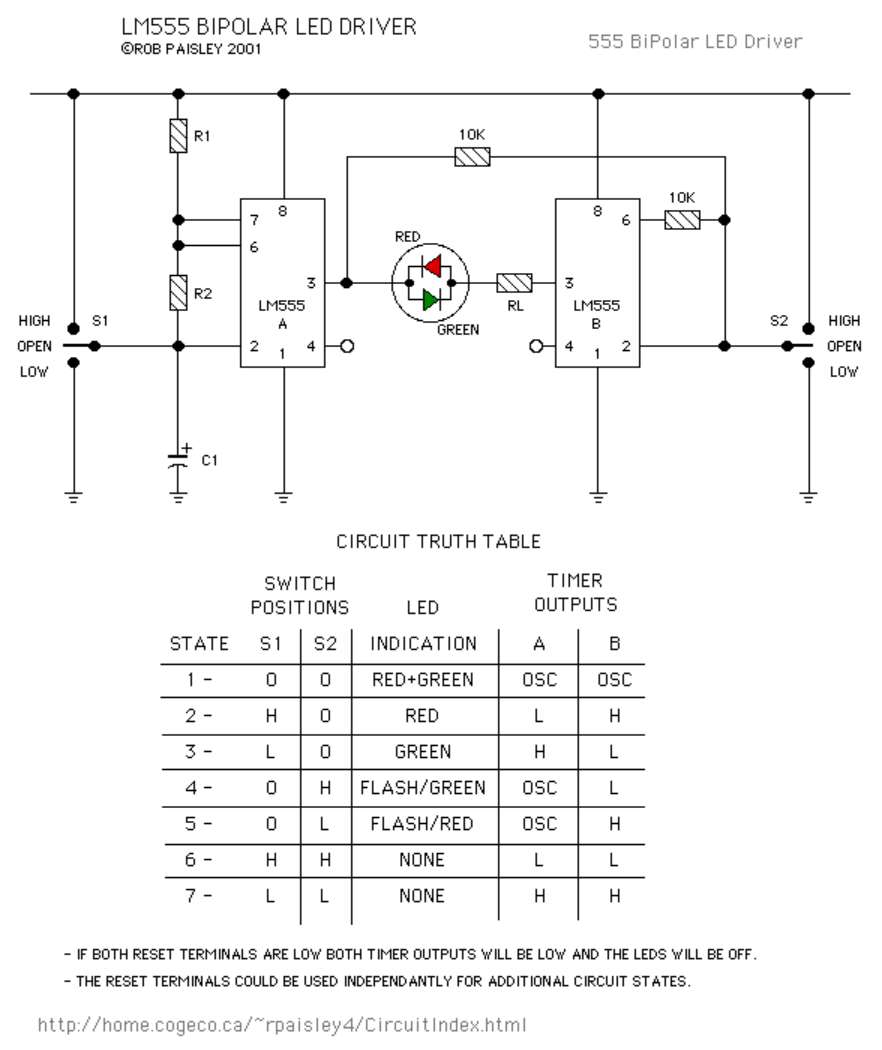
## Bipolar LED Driver

This circuit uses two timers to drive Bipolar LEDs and shows all of the possible output states.

Two SPDT switches are used to set the input conditions but these could be replaced by electronic controls.




| | SWITCH POSITIONS | | LED | TIMER OUTPUTS | |
|---|---|---|---|---|---|
| STATE | S1 | S2 | INDICATION | A | B |
| 1 - | 0 | 0 | RED+GREEN | OSC | OSC |
| 2 - | H | 0 | RED | L | H |
| 3 - | L | 0 | GREEN | H | L |
| 4 - | 0 | H | FLASH/GREEN | OSC | L |
| 5 - | 0 | L | FLASH/RED | OSC | H |
| 6 - | H | H | NONE | L | L |
| 7 - | L | L | NONE | H | H |

- IF BOTH RESET TERMINALS ARE LOW BOTH TIMER OUTPUTS WILL BE LOW AND THE LEDS WILL BE OFF.
- THE RESET TERMINALS COULD BE USED INDEPENDANTLY FOR ADDITIONAL CIRCUIT STATES.

http://home.cogeco.ca/~rpaisley4/CircuitIndex.html

**Bipolar LED Driver schematic**

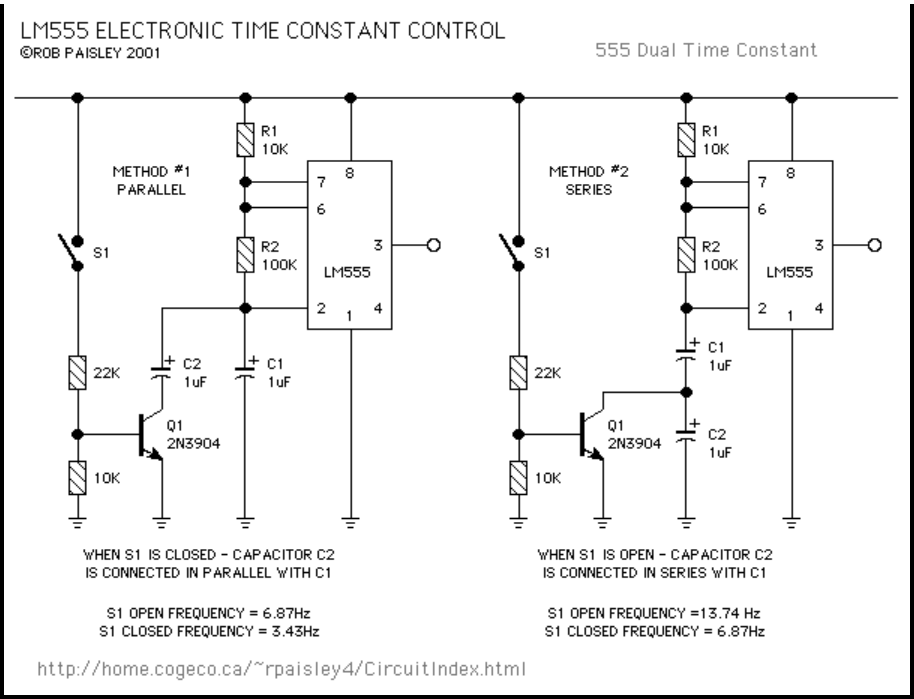
RESET And CONTROL Input Terminal Notes

---

# Electronic Time Constant Control

These circuits show methods of changing the operating frequency of astable LM555 timers electronically. Any source that can drive the base of transistor Q1 can control these circuits.

The advantage of switch the timing capacitors is that the duty cycle of the timer is not affected when the frequency is changed.




**Electronic Time Constant Control**

RESET And CONTROL Input Terminal Notes

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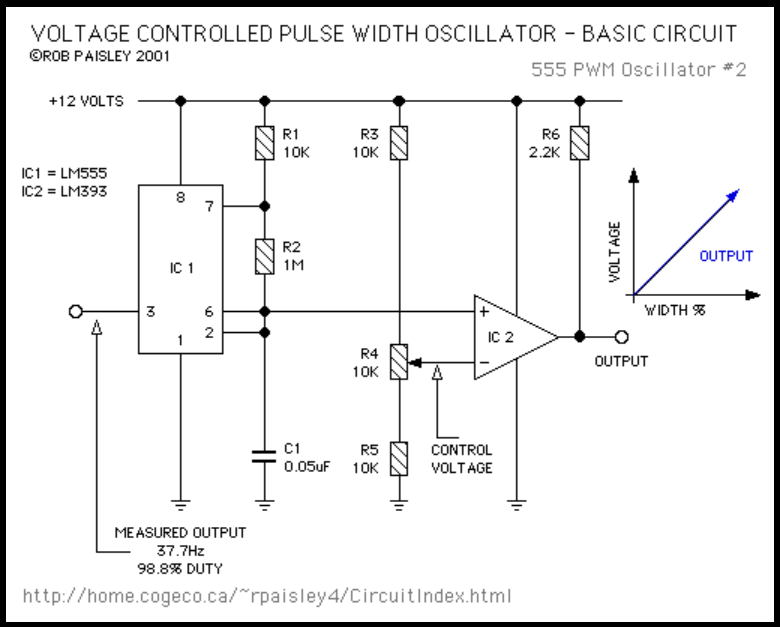
# Voltage Controlled Pulse Width Oscillator

The basic circuit operates at a frequency determined by R1, R2 and C1 and has a pulse width range of 0 to 100 percent.

The following diagram shows a basic circuit with an open collector output that would require a pull up resistor at its output. The parts values are the nominal values of the components used.

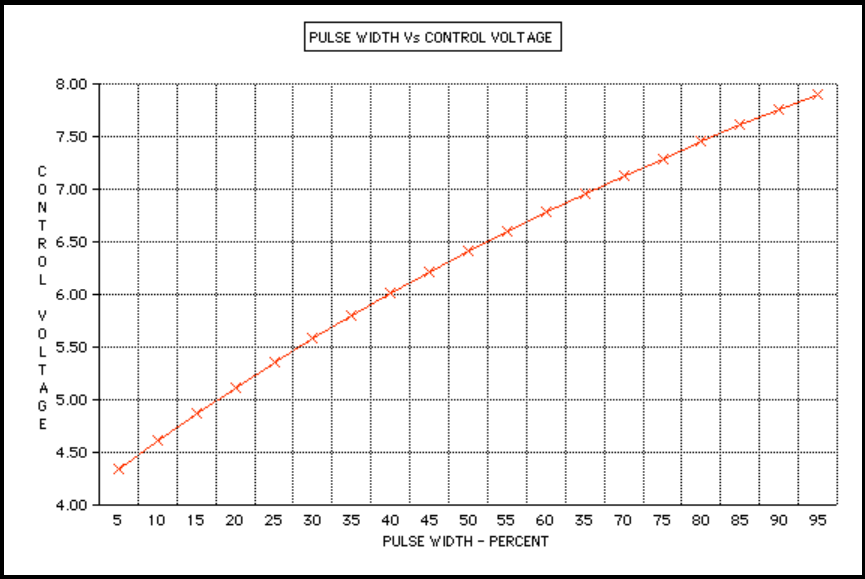
**Note: This circuit is not suitable for high frequency operation, especially when using a second timer as the output stage.**




**Variable Pulse Width Oscillator**

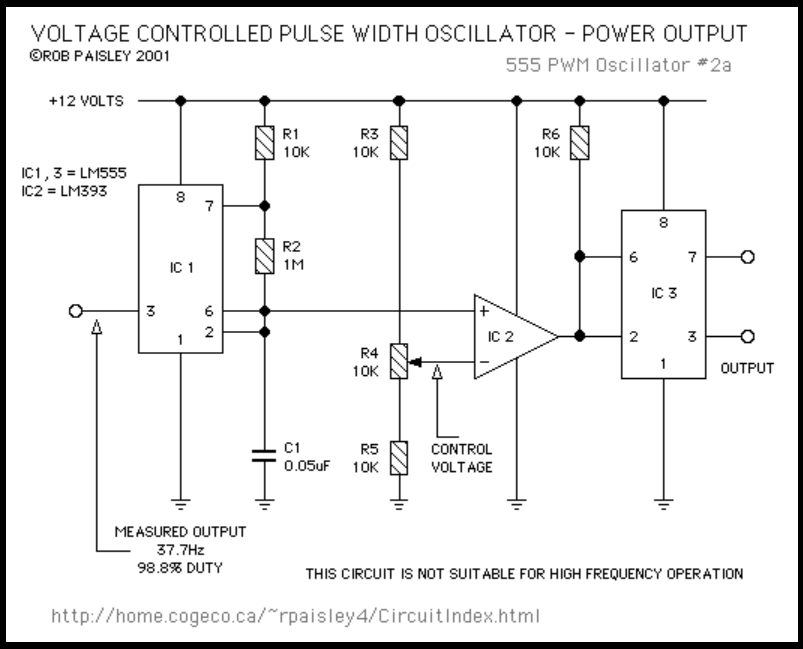
The following is a graph of the output pulse width of the basic circuit for a given control voltage input. All measurements were made with a good quality multimeter.

The PLUS and MINUS inputs of IC 2 can be reversed to produce a decreasing pulse width for an increasing control voltage.




**Variable Pulse Width Oscillator Output Graph**

The next diagram uses a second LM555 timer as a power output stage for the basic oscillator. The output stage also has an open collector output at the Discharge terminal, PIN 7, that could be used.




**Variable Pulse Width Oscillator With LM555 Output**

RESET And CONTROL Input Terminal Notes

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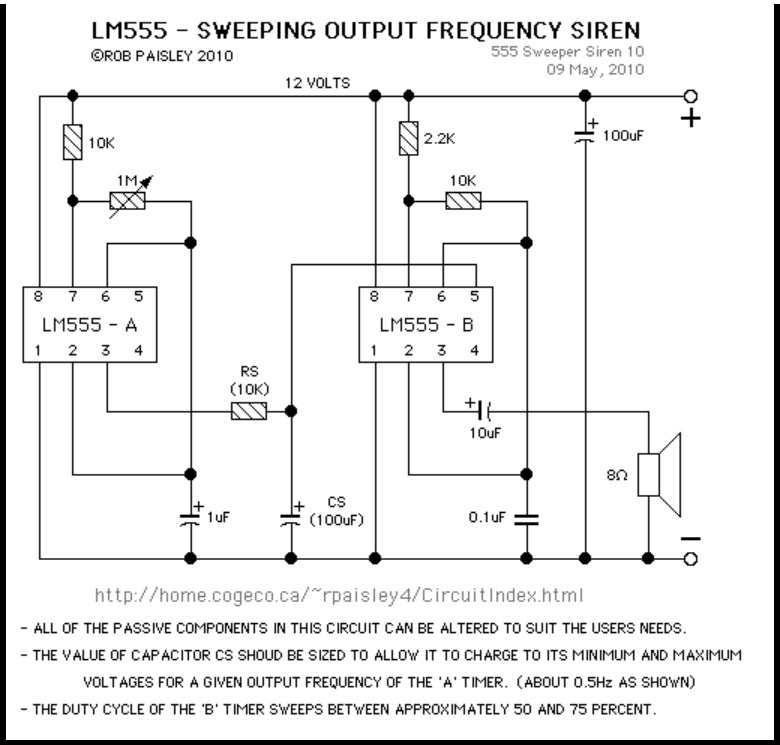
# Sweeping Output Siren

This circuit is a variation of the "Two Tone Siren" that is a standard for the LM555 timer. The circuit allows the output frequency of the B timer to sweep between two frequencies rather than switching abruptly between two frequencies.




**Sweeping Output Siren**

NOTE: The Sweeping Output Siren circuit has a limited sweep range and the duty cycle shifts with the changing output frequency.

A better 555 based circuit for a sweeping oscillator would be to adapt the Variable Pulse Width Oscillator in the section above.

A still better choice for a sweeping oscillator would be a Voltage Controlled Oscillator (VCO) IC. See this Wikipedia page for basic information on Voltage-controlled oscillators and this datasheet for the LM321.

Other devices include the TTL 74124 Dual Voltage-Controlled Oscillator and the CMOS CD4046B Phase-Locked Loop.

RESET And CONTROL Input Terminal Notes

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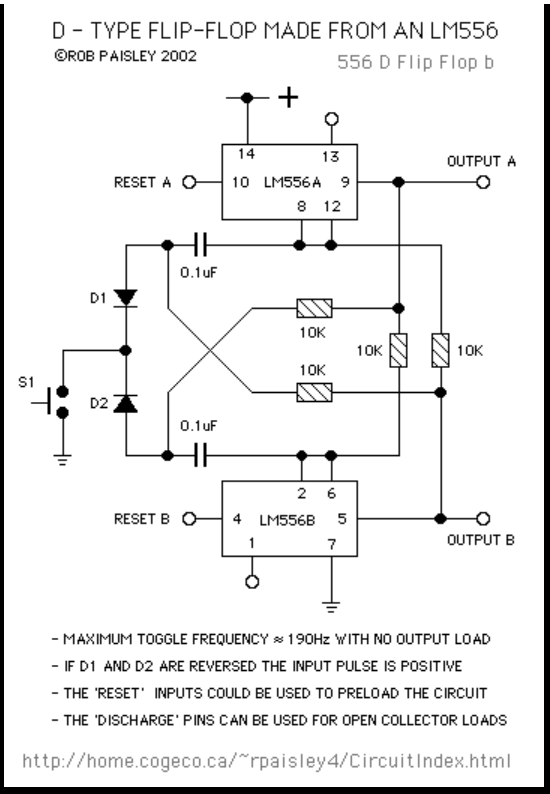
# D Type Flip-Flop Made With A LM556 Timer

This circuit is a hybrid - D type Flip-Flop that is constructed from an LM556 - Dual Timer integrated circuit. The circuit is essentially an expensive version of the classic - two transistor Flip-Flop but it does have an output current capacity of 200 milliamps.

Each time the push button switch (S1) is closed the outputs of the timers will reverse so that one is HIGH and the other is LOW and vice versa. As with the D flip-flop the circuit acts as a binary divider.




**D - Flip-Flop**

The circuit has some output switching time lag due to the RC time constants at the inputs and the different Trigger and Threshold voltage levels of the timers themselves.

RESET And CONTROL Input Terminal Notes

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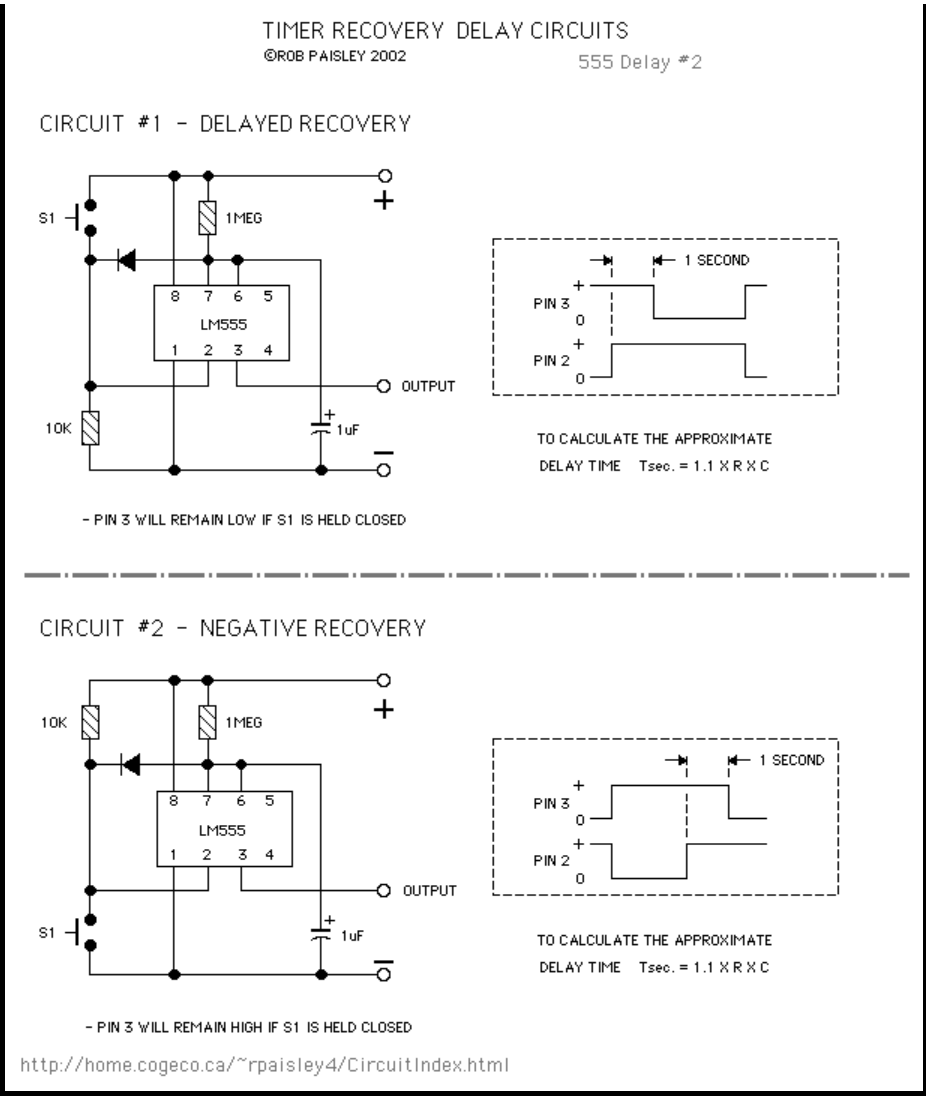
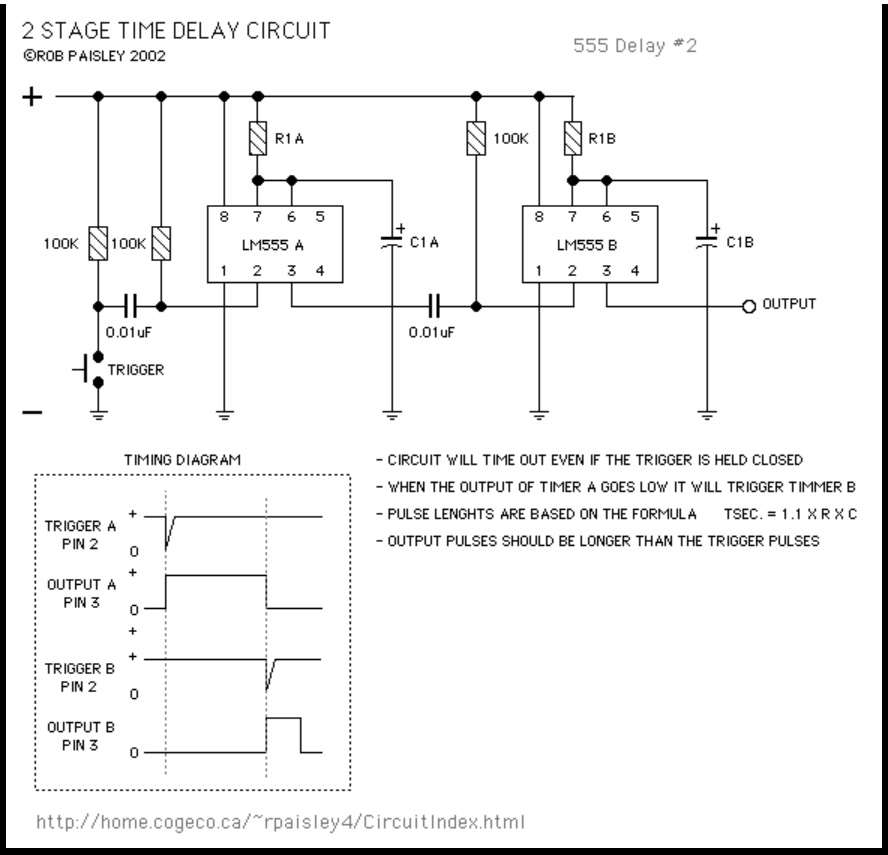
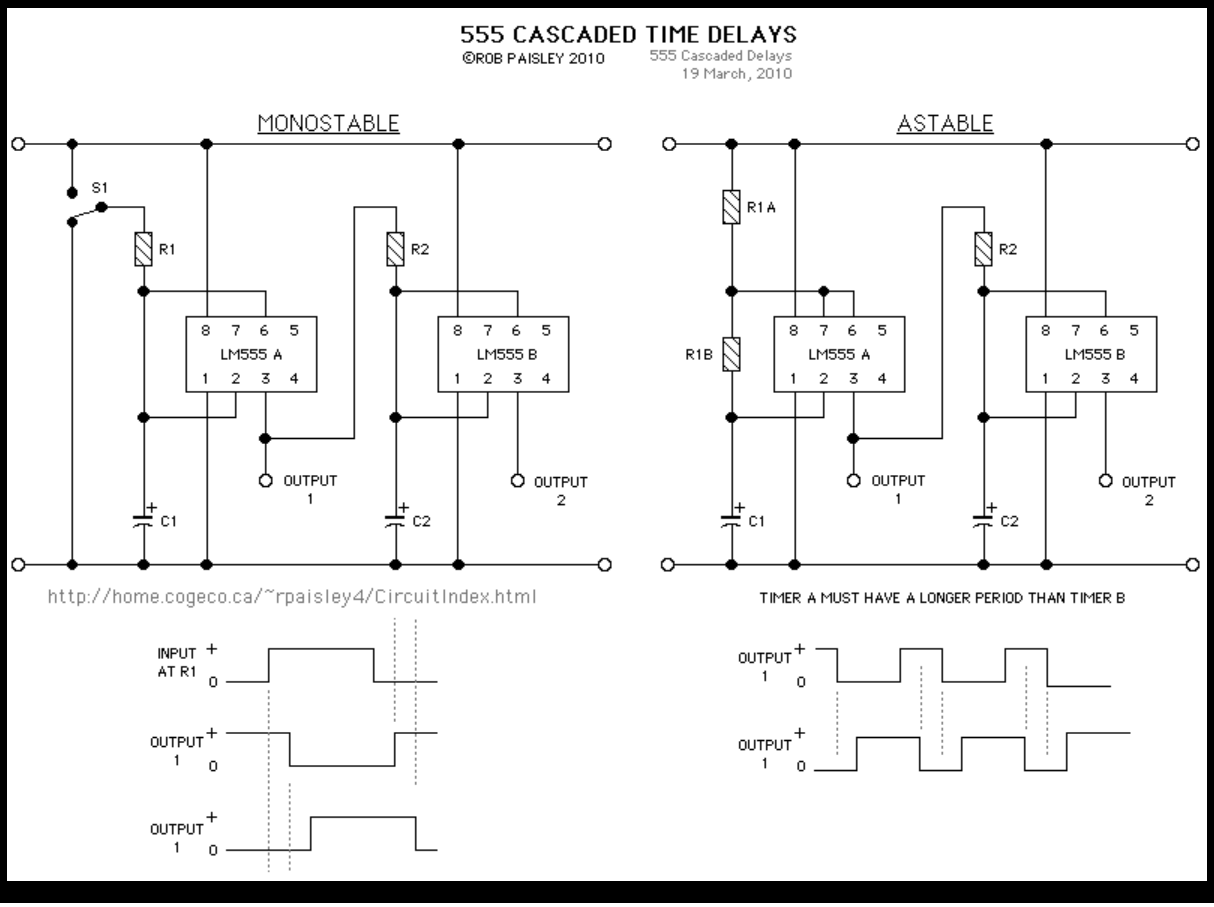
## Time Delay Circuits - Various




**Time Recovery Delay Circuits**

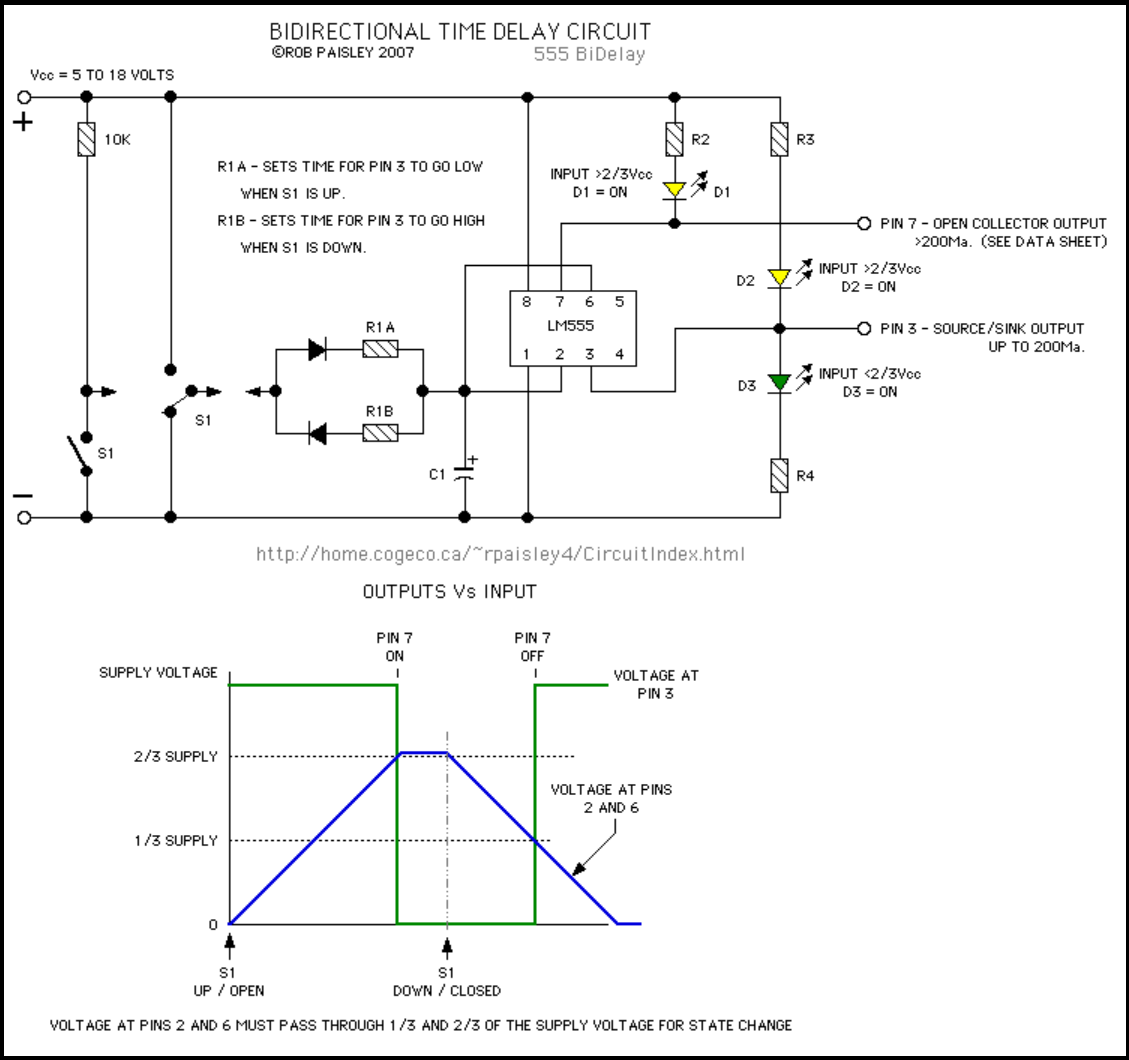



**Two Stage Time Delay Circuit**



**Cascaded Time Delay Circuits**

## Example Circuit - 4 Stage Cascade Delay




**BiDirectional Time Delay Circuit**

In the BiDirectional Time Delay Circuit, the B timer acts more as a Schmitt trigger with a delay than a conventional timer. See section 13 of this page for more detail.

RESET And CONTROL Input Terminal Notes

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# Variable period Oscillator (CD4017)

**The following CD4017 circuits have not been tested and is presented here as a possibility only. If you experiment with this circuit, please send me any problems found so that the circuit can be updated.**

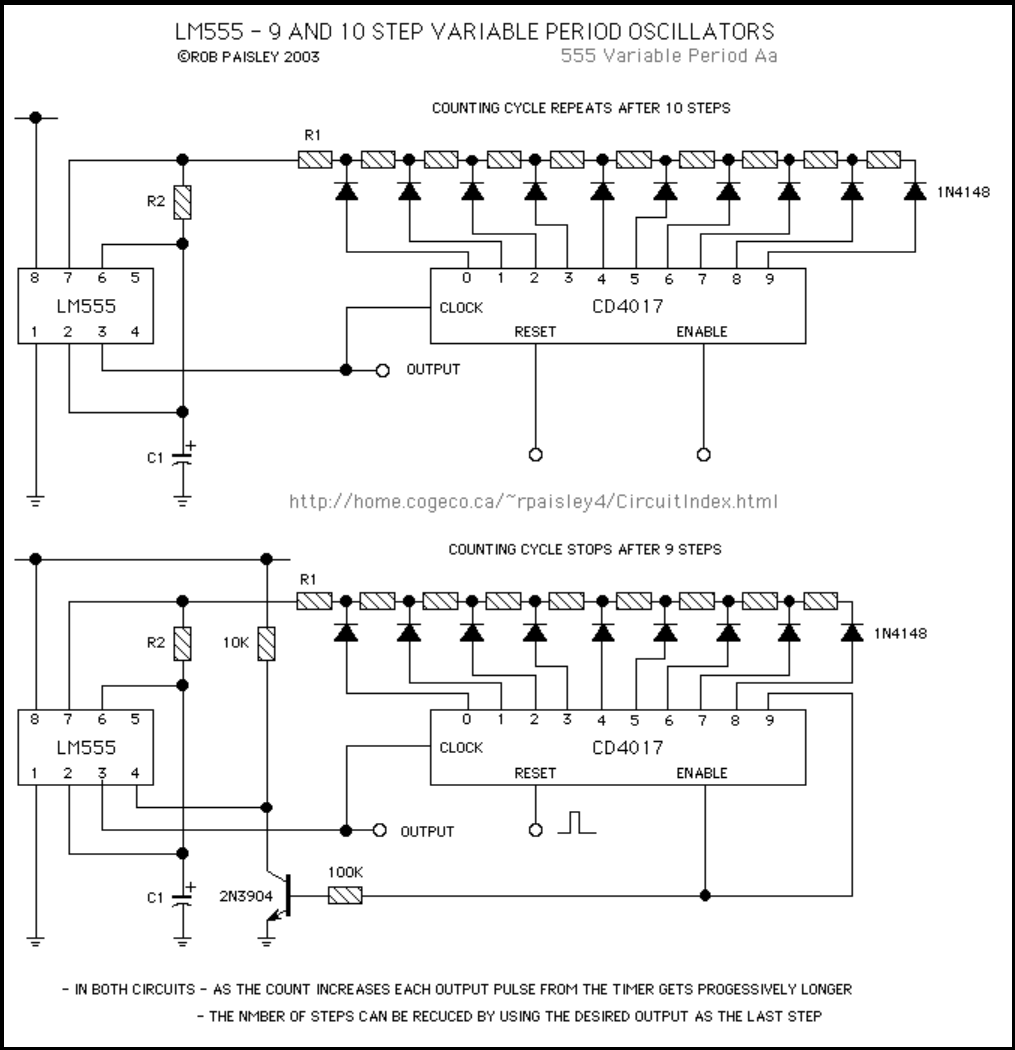
The following circuits are designed to change the duration of each positive output pulse from the astable timer. The circuits use a CD4017 Decade Counter / Decoder to provide nine or ten steps in the cycle.

The first circuit operates with a repeating ten step cycle. Each output pulse is longer than the previous until a count of ten is reached at which time the cycle will repeat.

The second circuit has a nine step cycle that stops at the end of the cycle. The cycle is restarted or reset when the RESET input is briefly made high.

The CD4017 can be configured to give count lengths between 1 and 10. Refer to the timing diagram in the CD4017 data sheet for a better understanding of the IC's operation.

**CD4017 Data sheet - National Semiconductor (.pdf)**




**Variable Period Oscillator (Experimental)**

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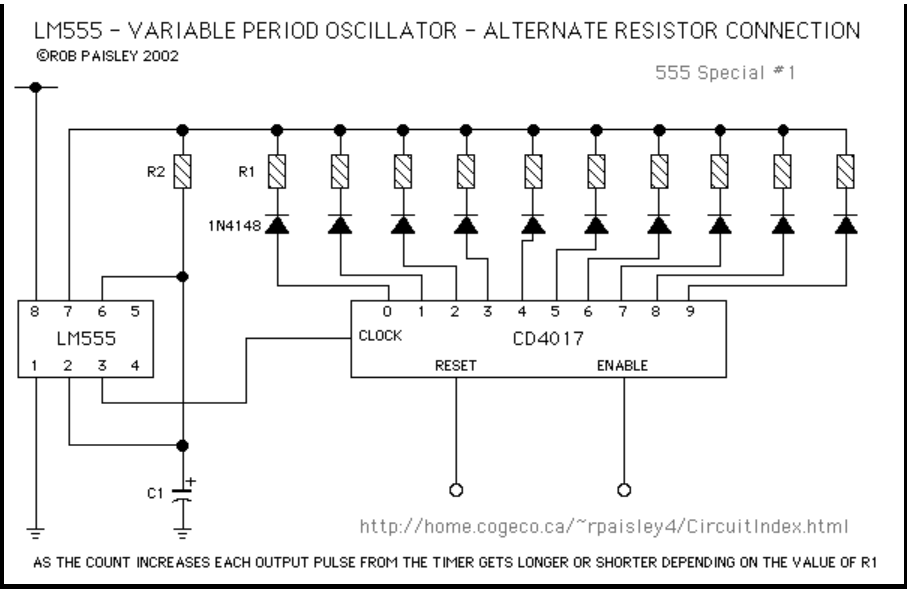
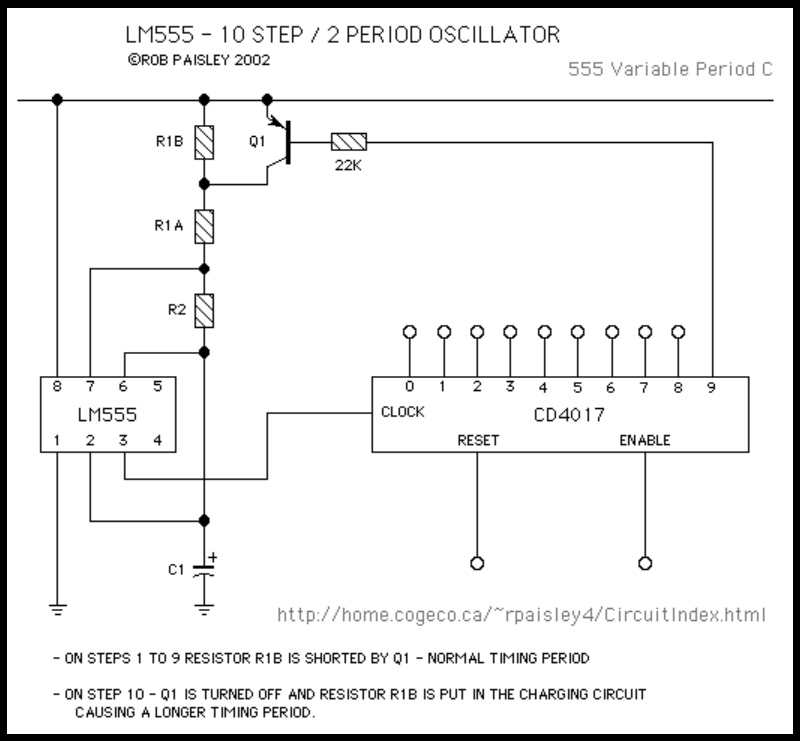
The next schematic shows an alternate arrangement for the timing resistors. This would allow the subsequent output pulses to be of longer and shorter lengths during the cycle.




**Alternate Resistor Arrangement**

The next circuit provides nine counts of a normal timing length with the tenth count being longer and then repeating the cycle.




**Ten Step / Two Period Oscillator**

RESET And CONTROL Input Terminal Notes

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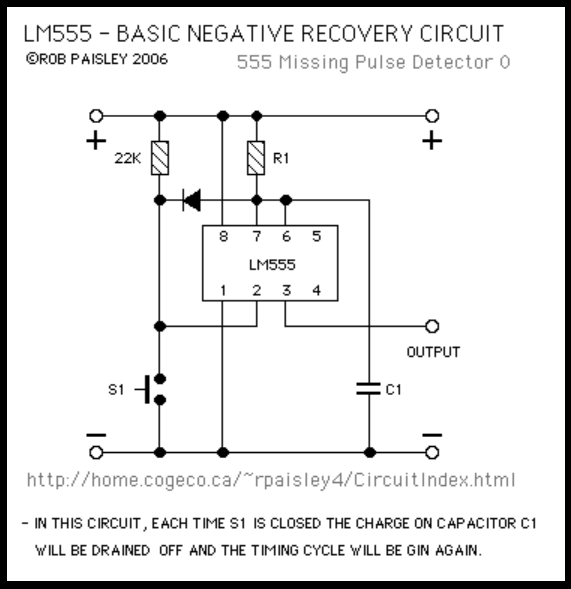
## Missing Pulse Detector / Negative Recovery Circuits

**Basic - Negative Recovery Circuit**

The first circuit is a simple, push button controlled, Negative Recovery timer circuit. Each time that S1 is closed the time

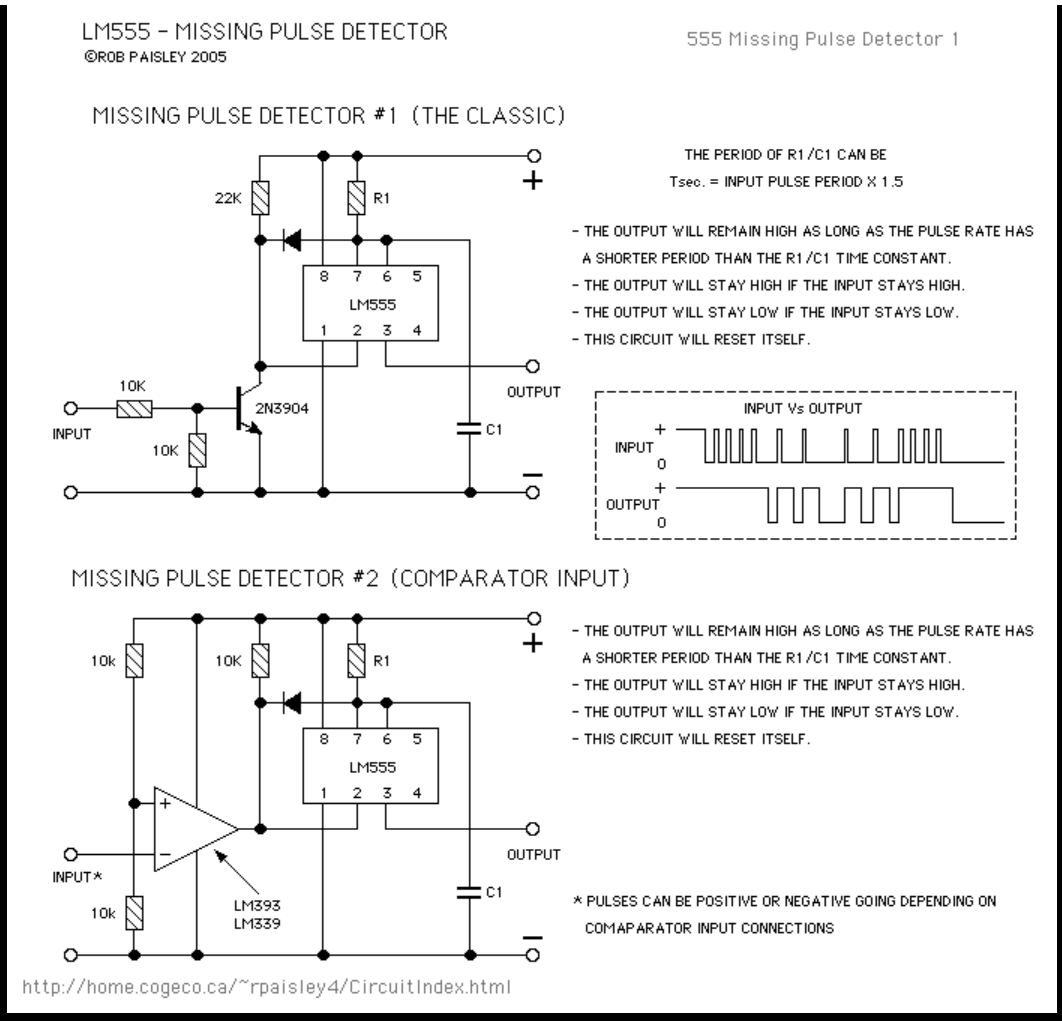
remaining in the cycle is reset to zero. If the time does run out, closing S1 will restart the cycle.



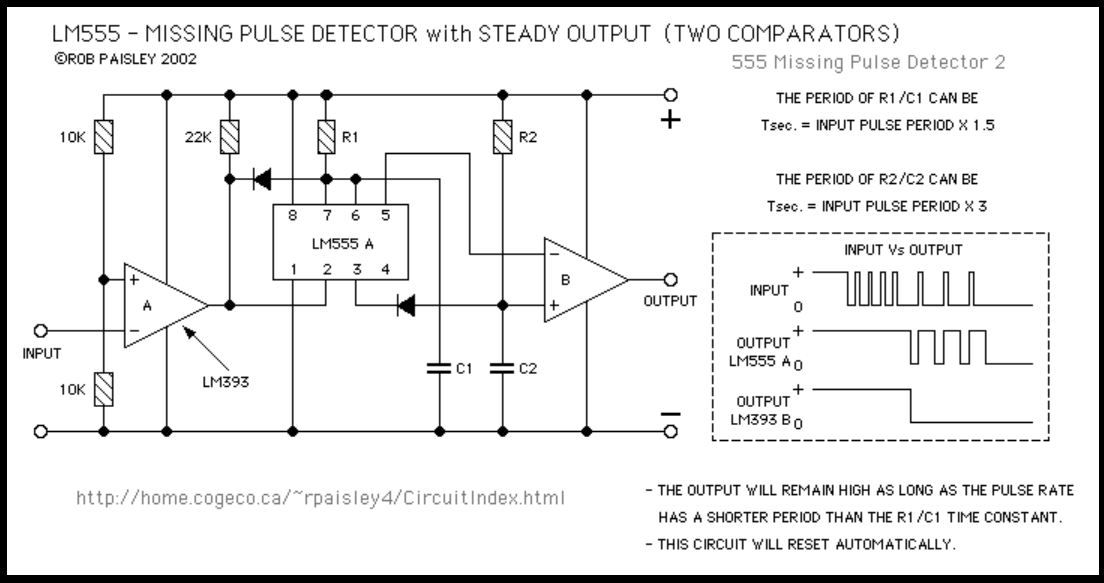

The following circuits can detect when a train of pulses stops or become too far apart. They can also be use to keep the timer at its zero count if the input is held in a steady state. This is called 'Negative Recovery'.

The diode across R1 in these circuits causes C1 to quickly discharge when the power to the circuit is switched off. This allows the circuit to be ready for the next cycle more quickly.

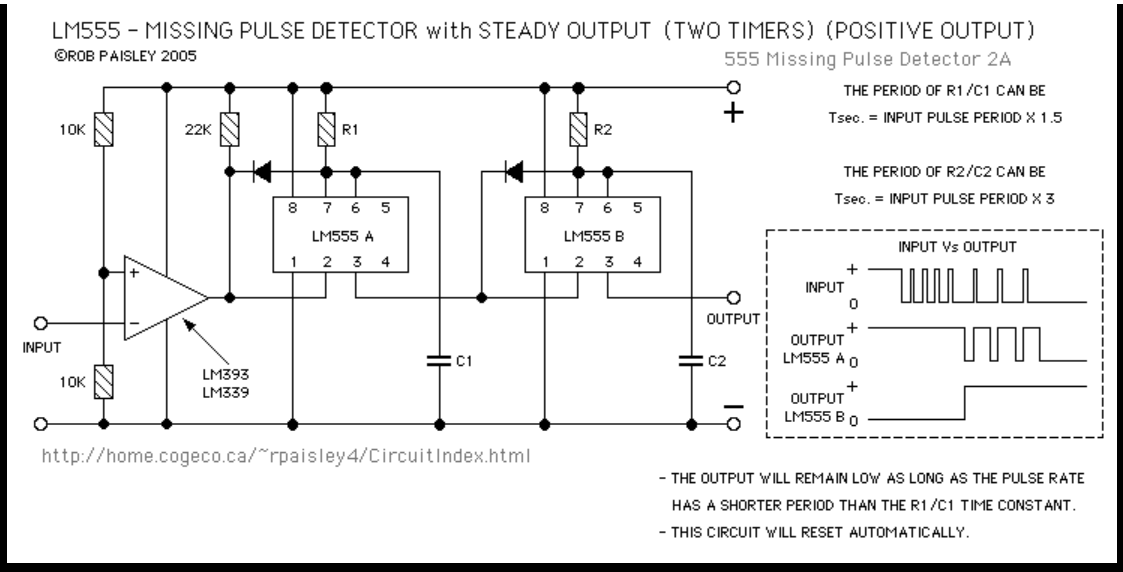
**Basic - Missing Pulse Detectors**




**Steady Output - Missing Pulse Detectors - Two Comparators**

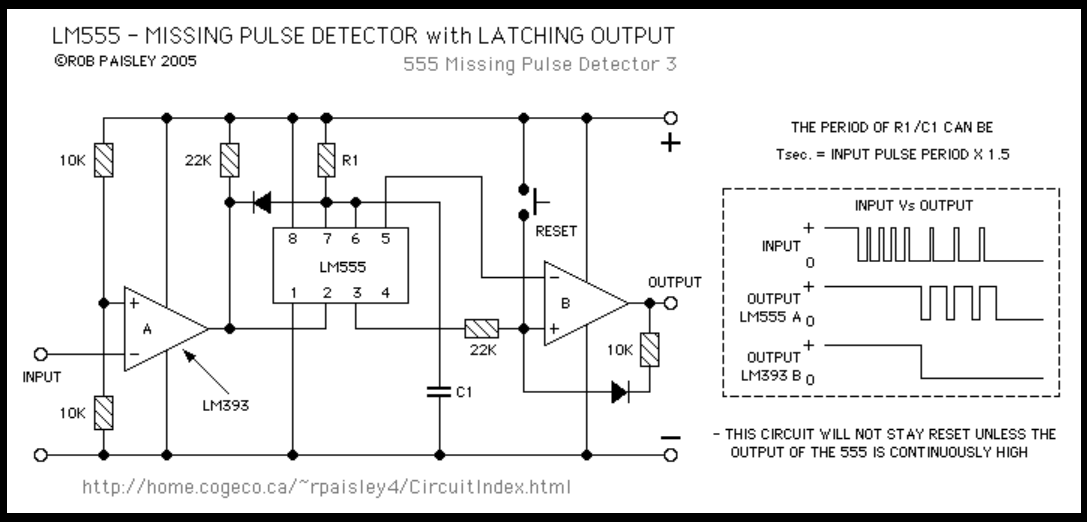



**Steady Output - Missing Pulse Detectors - Two Timers**

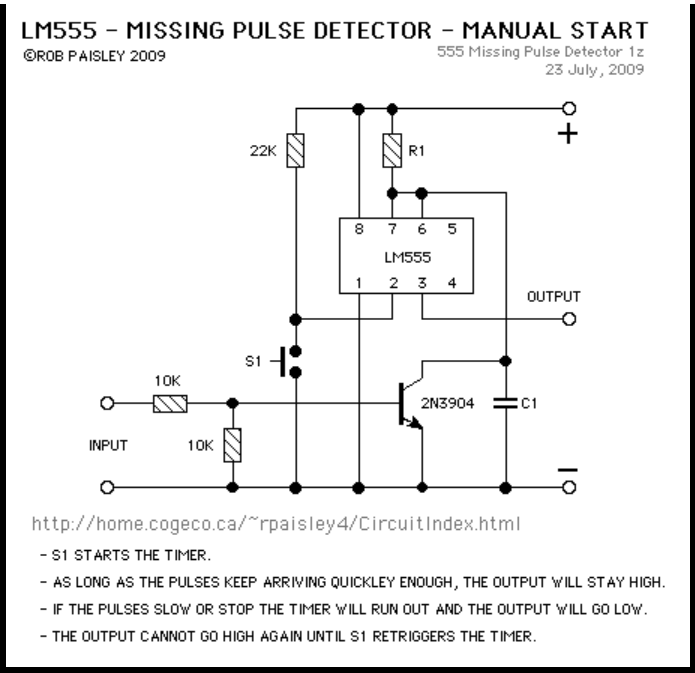



The next two circuits in this section produce the same result: The timer must be reset manually if it has timed out.

**Latching Output - Missing Pulse Detector**




**Manual Start - Missing Pulse Detector**

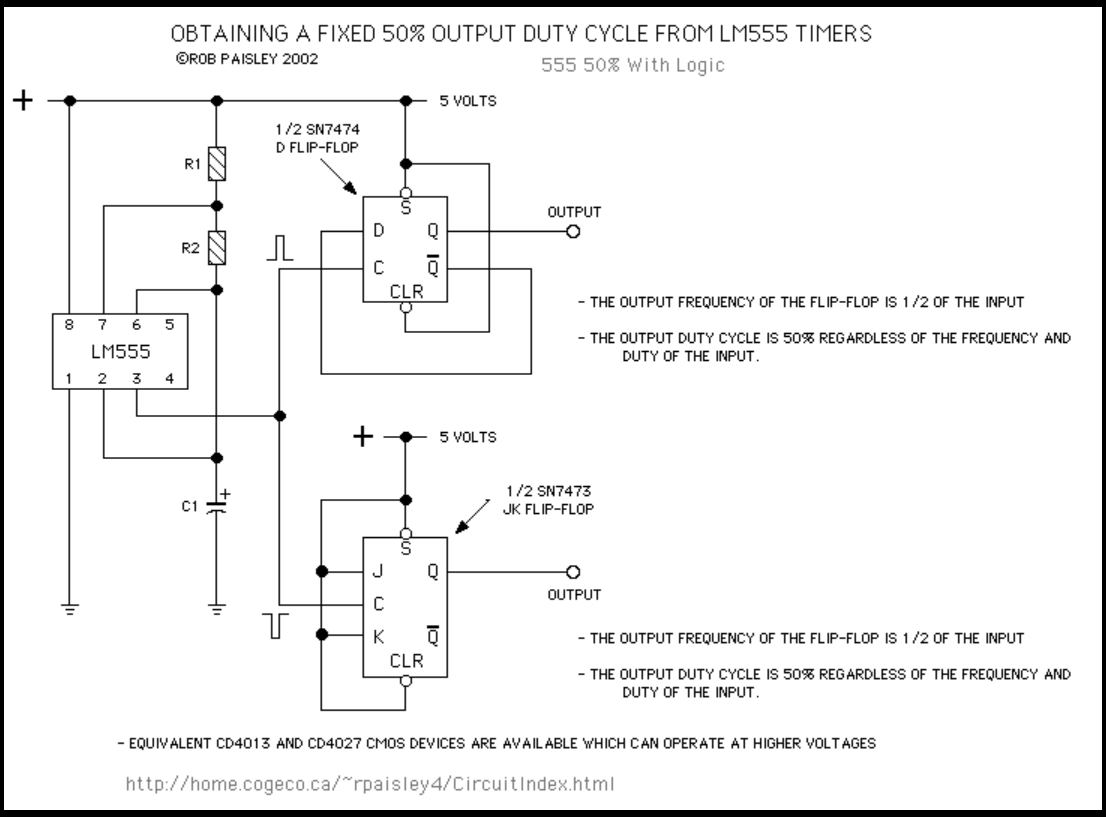



RESET And CONTROL Input Terminal Notes

## Fixed 50% Output Duty Cycle Using Logic Devices

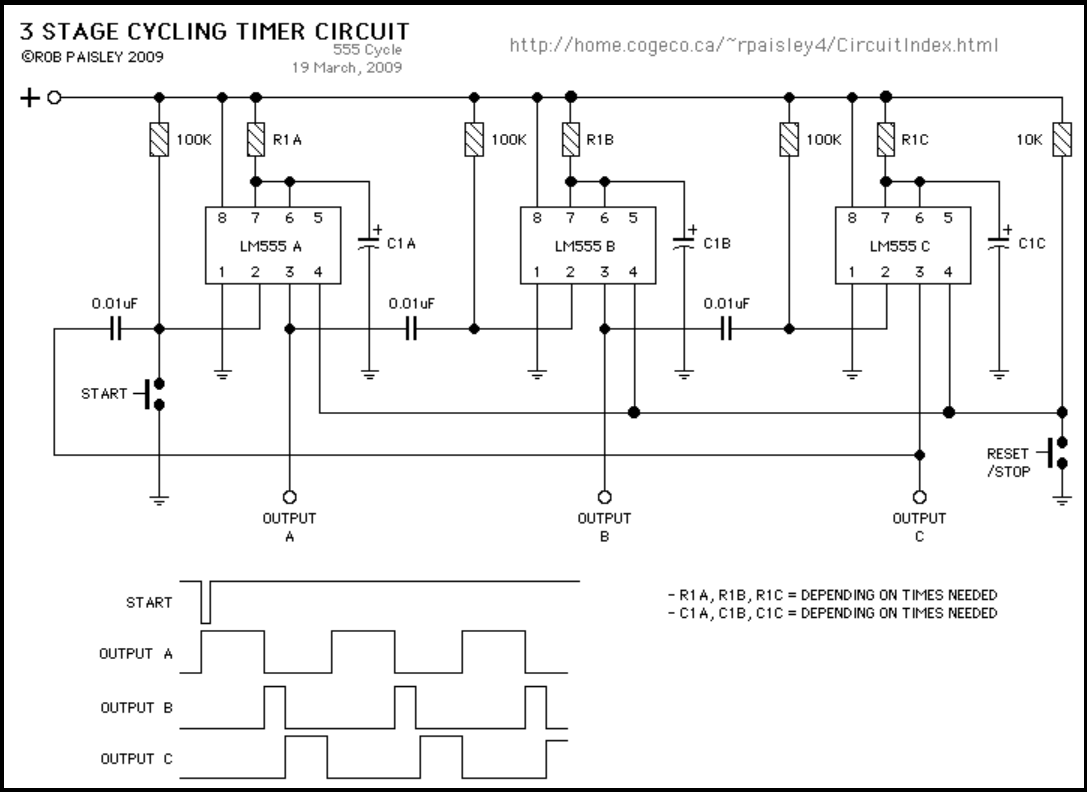
The only way to achieve a true - 50 percent duty cycle from a 555 timer is to divide the output by 2 with a binary divider such as the 7473 or 7474 TTL logic ICs.

**Fixed 50% Output Duty Cycle**



RESET And CONTROL Input Terminal Notes

## Three Stage - Cycling Timer Circuit




**NOTE** All three timers in this circuit will start when power is applied, therefore all but the first timer (A) will need to be Reset for the proper cycle order to be started automatically. (See item 10 in the index of this page for a method of resetting the timers.)

### A Single - Traffic Light Driver Circuit - Based On The Cycling Timer Circuit

RESET And CONTROL Input Terminal Notes

**Devices Used For The Following Tests**


## RESET Terminal - Currents And Voltages

The next diagram gives the current from, and the voltage at the RESET terminals of five - 555 timer chips from different manufacturers.

The only conclusion to be drawn here is that the RESET terminal should be held below 0.3 Volts to ensure that any of the devices is fully reset.

In the transition voltage range of the RESET terminal mentioned on the diagram, the timers output is neither fully ON or OFF. This can cause high current flows in the timer itself. The voltage at the RESET terminal should pass through this range as quickly

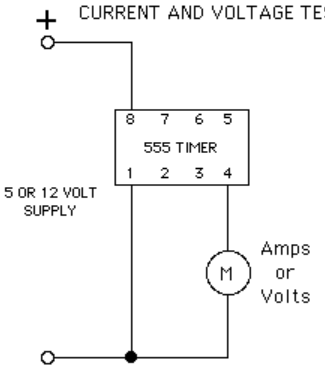
as possible to avoid problems.

**RESET Terminal - Currents And Voltages**

LM555 TIMER - RESET TERMINAL CURRENT AND VOLTAGE VALUES

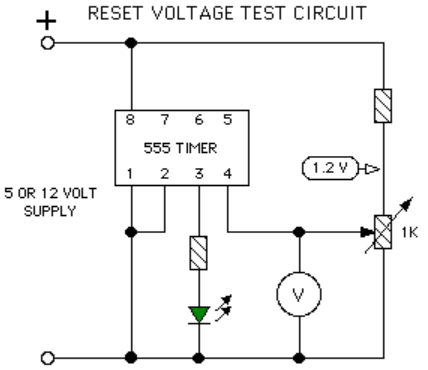


555 Reset Terminal




| DEVICE | RESET TERMINAL CURRENT (uA) @5 VOLTS | RESET TERMINAL CURRENT (uA) @12 VOLTS | RESET TERMINAL VOLTS (TERMINAL OPEN) @5 VOLTS | RESET TERMINAL VOLTS (TERMINAL OPEN) @12 VOLTS |
|---|---|---|---|---|
| LMP555CN | 19.3 | 65.9 | 0.26 | 0.34 |
| CA555CE | 14.7 | 82.0 | 0.88 | 0.98 |
| UA555TC | 63.5 | 185.5 | 0.92 | 1.00 |
| NE555P | 12.0 | 51.5 | 0.83 | 0.92 |
| MC1455P1 | 17.8 | 111.0 | 0.86 | 0.98 |

http://home.cogeco.ca/~rpaisley4/CircuitIndex.html




| DEVICE | RESET VOLTAGE* @5 VOLTS | RESET VOLTAGE* @12 VOLTS |
|---|---|---|
| LM555CN | 0.51 | 0.46 |
| CA555CE | 0.50 | 0.46 |
| UA555TC | 0.37 | 0.34 |
| NE555P | 0.41 | 0.37 |
| MC1455P1 | 0.47 | 0.42 |

* - VOLTAGE AT WHICH THE LED WAS COMPLETELY DARK (EACH DEVICE HAD A SMALL DEADBAND VOLTAGE WHERE THE OUTPUT WAS IN TRANSITION)

RESET And CONTROL Input Terminal Notes

## 555 Timer Current Draws

The next diagram shows the basic current consumption of 555 timer chips from different manufacturers.

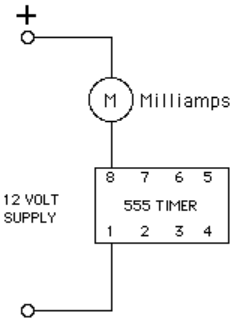
The RESET terminal current draw illustrates the need for a current limiting resistor as shown in some of the preceding circuits. Some devices will not function properly if the current to the THRESHOLD terminal is not restricted.

**Timer Current Draws**

LM555 TIMER - BASE LOAD CURRENT DRAWS



555 Current Draw

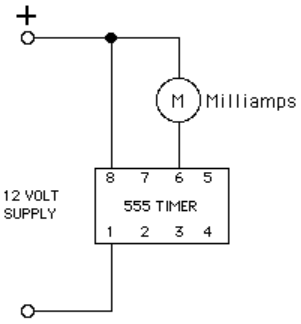



CURRENT DRAW TEST CIRCUIT

| DEVICE | CURRENT (mA) @5 VOLTS | CURRENT (mA) @12 VOLTS | RATIOS 2.4 |
|---|---|---|---|
| LMP555CN | 2.28 | 6.71 | 2.94 |
| CA555CE | 2.18 | 6.60 | 3.03 |
| UA555TC | 2.00 | 5.60 | 2.80 |
| NE555P | 1.94 | 5.06 | 2.61 |
| MC1455P1 | 2.78 | 6.58 | 2.78 |

BEST POSSIBLE RATIO 2.4 (12/5)

http://home.cogeco.ca/~rpaisley4/CircuitIndex.html




RESET CURRENT TEST CIRCUIT

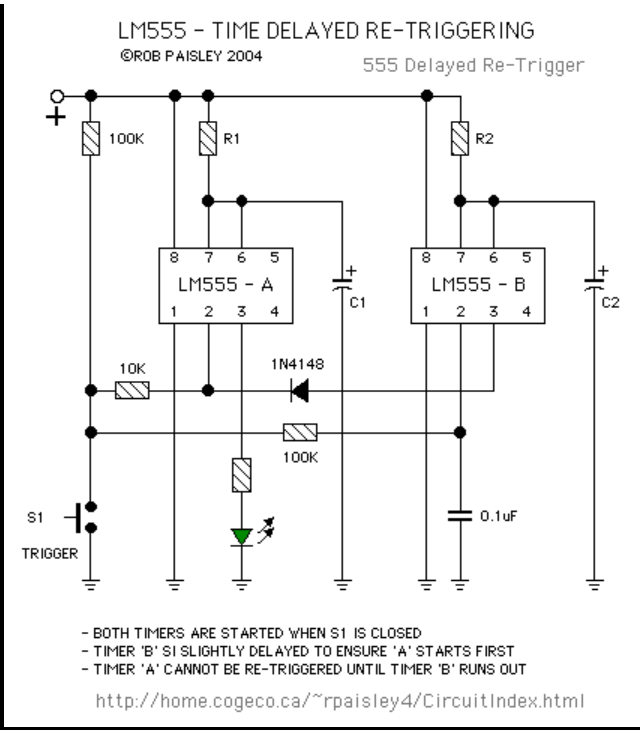
| DEVICE | CURRENT (mA) @12 VOLTS |
|---|---|
| LMP555CN | 1.67 |
| CA555CE | 2.67 |
| UA555TC | 3.30 |
| NE555P | 2.72 |
| MC1455P1 | 4.78 |

RESET And CONTROL Input Terminal Notes

## Delayed Re-Triggering

The following is a method of preventing a timer from being re-triggered before a certain time period has elapsed.

**Delayed Re-Trigger**




RESET And CONTROL Input Terminal Notes

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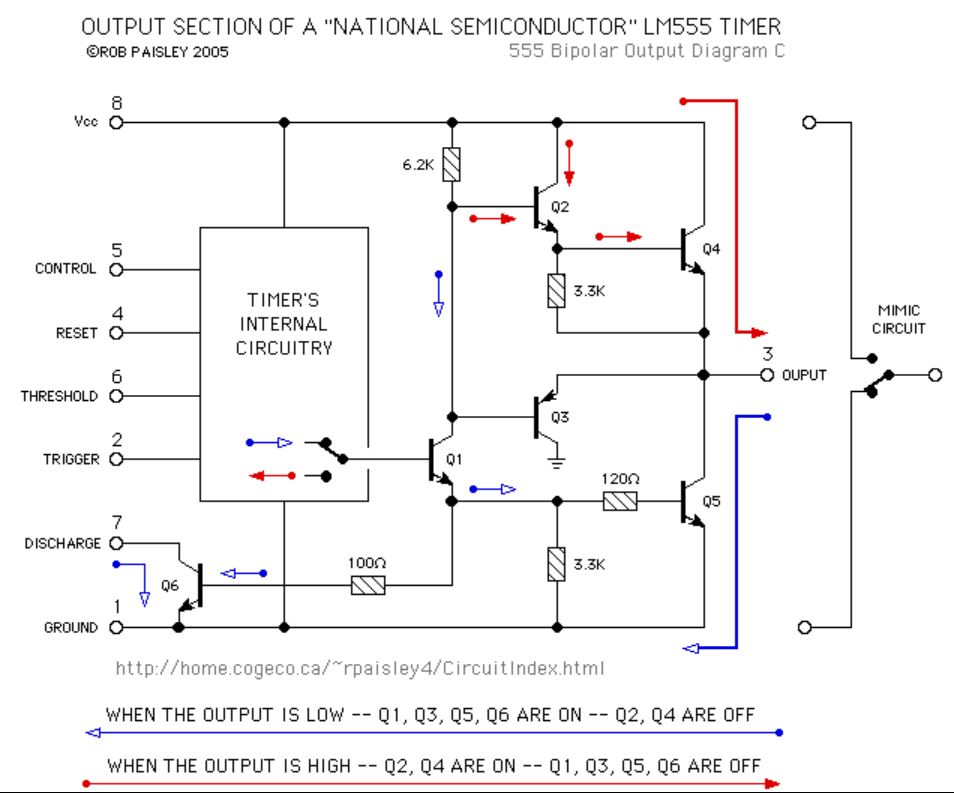
# Timer Output Section

The next diagram shows the output section of a National Semiconductor LM555 timer. This type of output can either source or sink current and is typical of 555 and 556 timer IC's.

When the output of the timer is HIGH, it can supply current to a load. When the output of the timer is LOW, it can receive current from a load.

Transistor Q3 is actually connected as a diode with the collector not carrying current. Although a circuit common symbol is shown, the collector is not connected to the ground of the timer.

**Output Circuit**




RESET And CONTROL Input Terminal Notes

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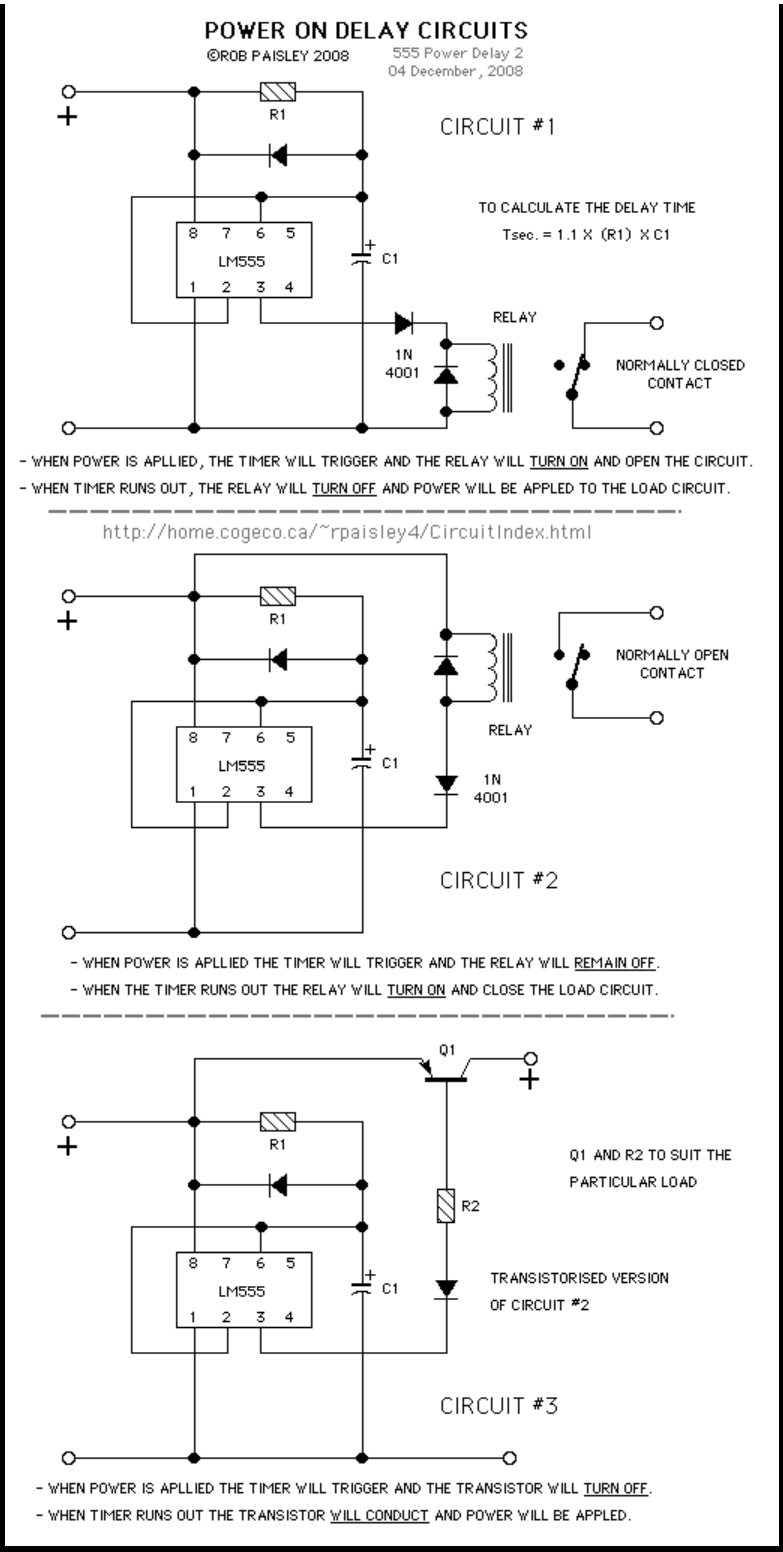
# Power ON Delay Circuits

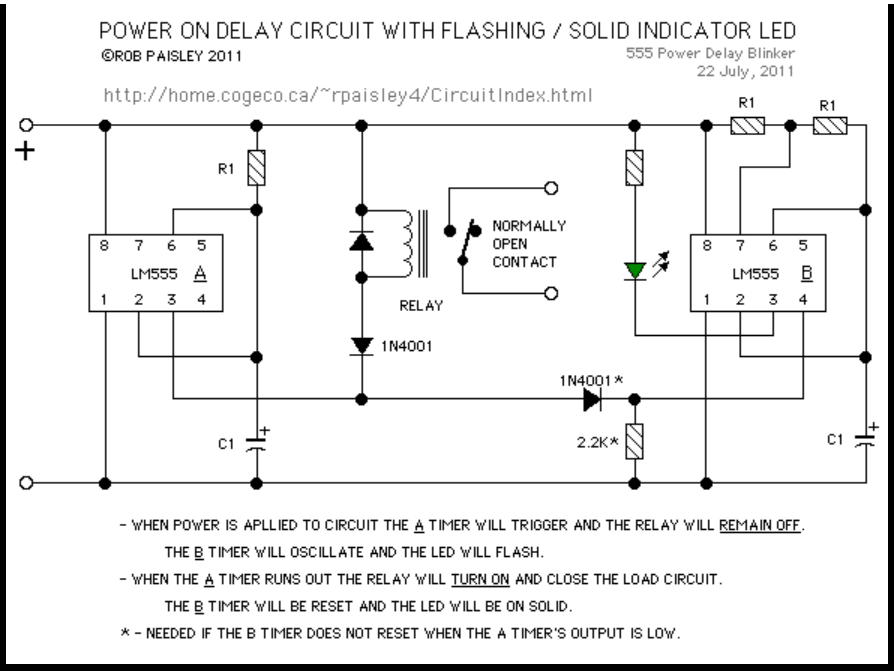
These circuits will delay the application of power to an external circuit by using mechanical relays or transistors. Other output control devices could also be used.

These circuits are not ideal as the relays are closed when power is supplied to the circuit. This means that the power is supplied to the load for a very short period until the relay can open.

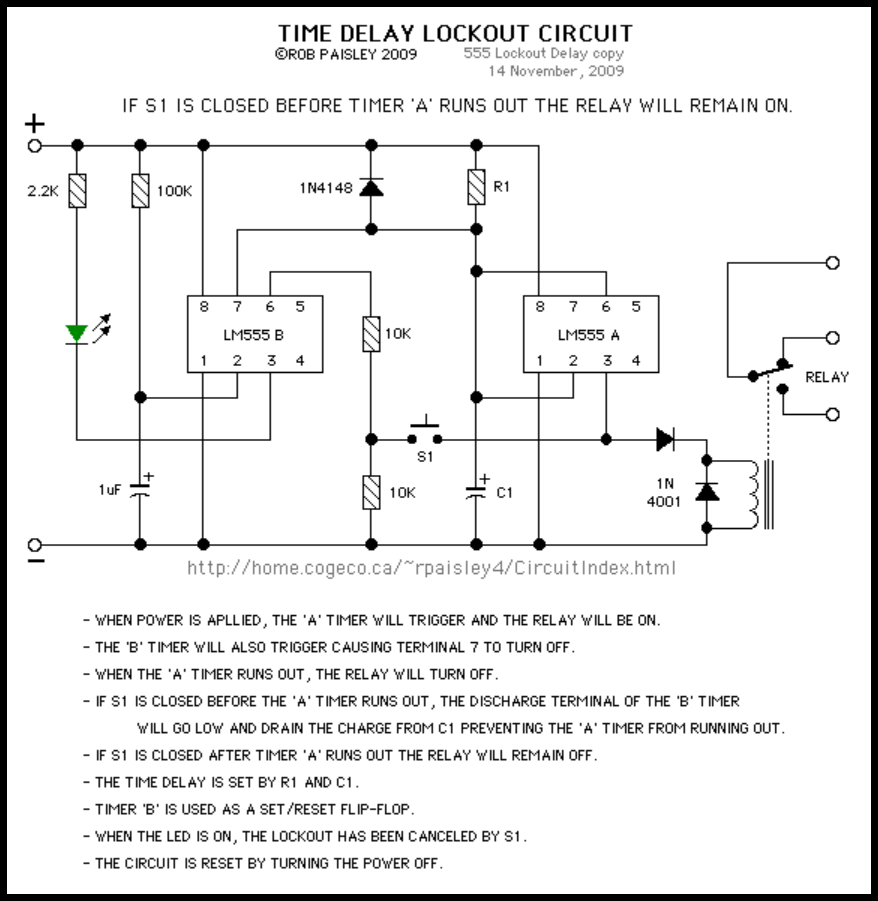
**Various Power ON Delay Circuits**




**Delay Circuit With Indicator LED**

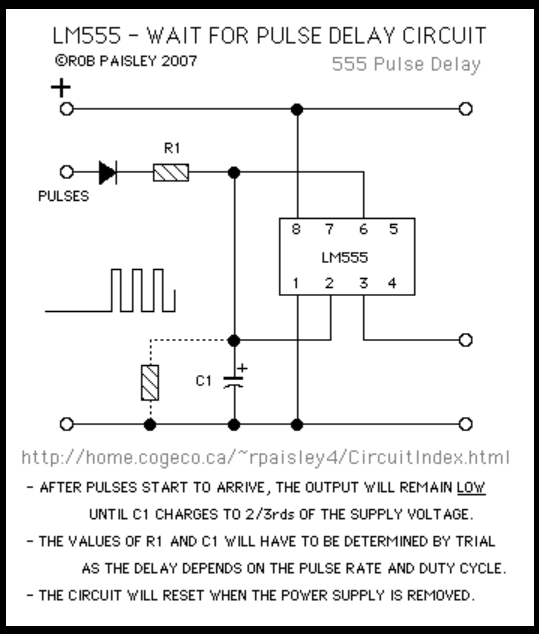



**Delayed Lock Out Circuit**




## PUJT & Voltage Comparator - Power On - Delay Circuits

**Wait For Pulses - Delay Circuit**




A variation on the Power On delay circuits above is a delay after pulses start arriving.

A resistor could be placed across capacitor C1 so that the timer will be reset if the pulses stop arriving. This resistor should have a resistance of at least three times the value of R1.

RESET And CONTROL Input Terminal Notes

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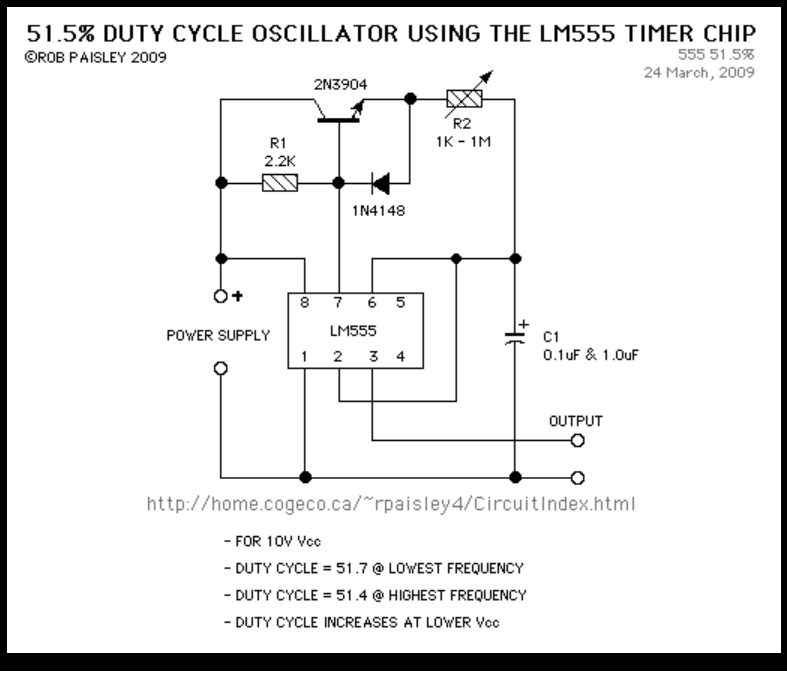
## Average 51.5 % Output Duty Cycle Using A 555 Timer

The next circuit produces an average duty cycle of 51.5% over the entire resistance range of R2 at a supply voltage of 10 volts.

At a supply voltage of 5 volts the average duty cycle increased to 52.7%. The span of the duty cycle also increased.

**51.5% Duty Cycle Oscillator**



RESET And CONTROL Input Terminal Notes

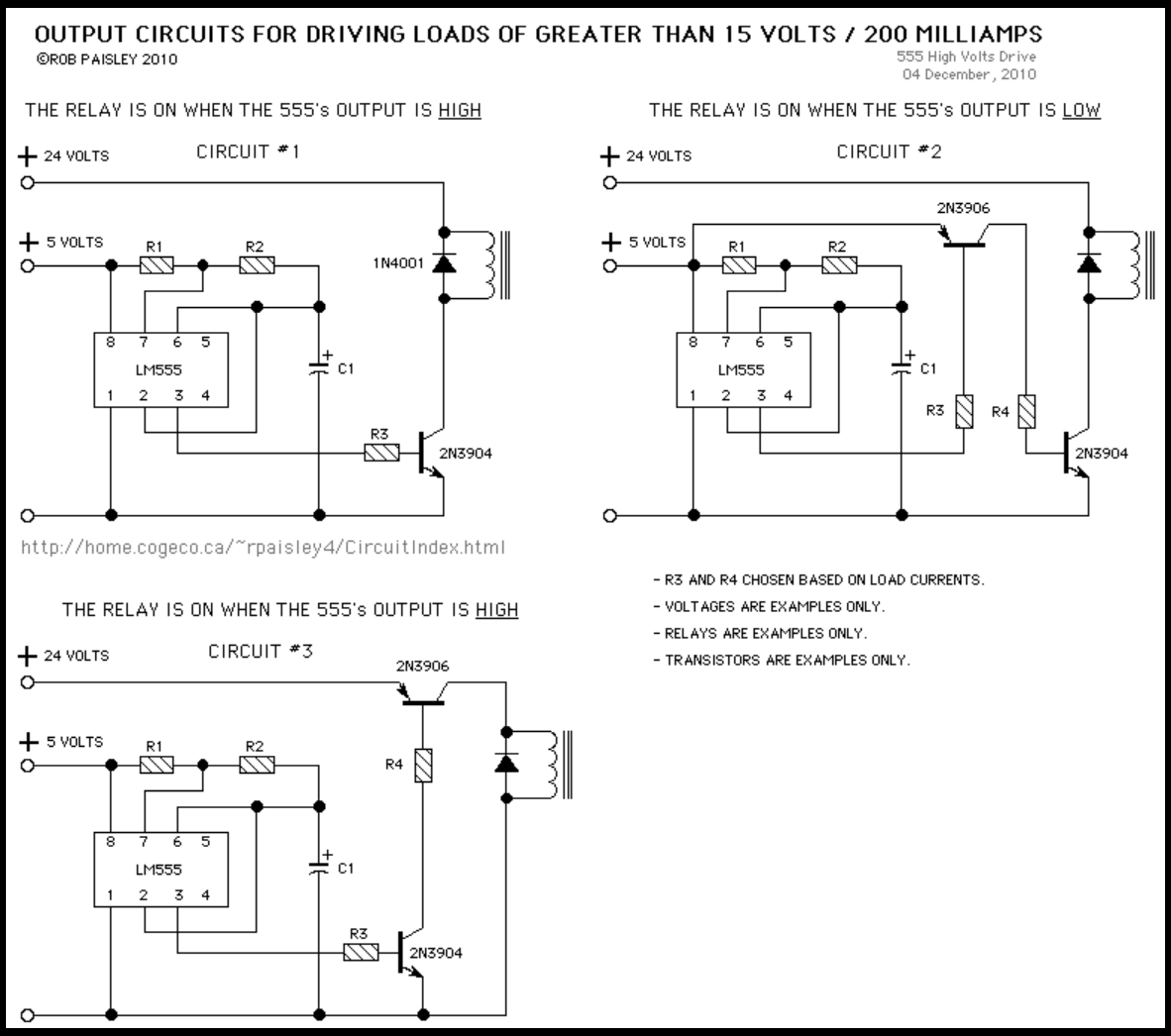
## Driving Loads Of Greater Than 15 Volts Or 200 Milliamps

The next two circuits allow the 555 timer to drive loads that have a supply voltage that is greater than the 15 volt maximum of 555 timers.

Higher current loads can be driven by transistors with a suitable current capacity and adjusting the base current as needed. Darlington and MOSFET transistors can drive loads of many amps.

The 24 volt supply can be full wave DC and does not need to be filtered. The load's supply voltage could also be lower than the timer's supply voltage.

**High Voltage And Current Load Drivers**

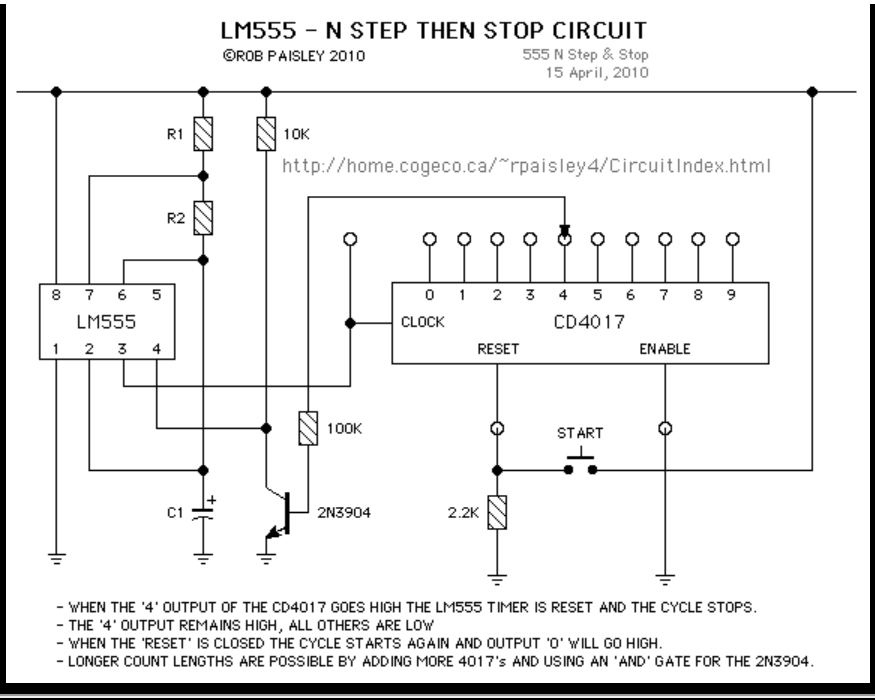



RESET And CONTROL Input Terminal Notes

## 'N' Steps And Stop Circuit (CD4017)

The next circuit uses the outputs of a CD4017 - Decade Counter to stop a 555 timer at a given step and then wait until the counter is reset.

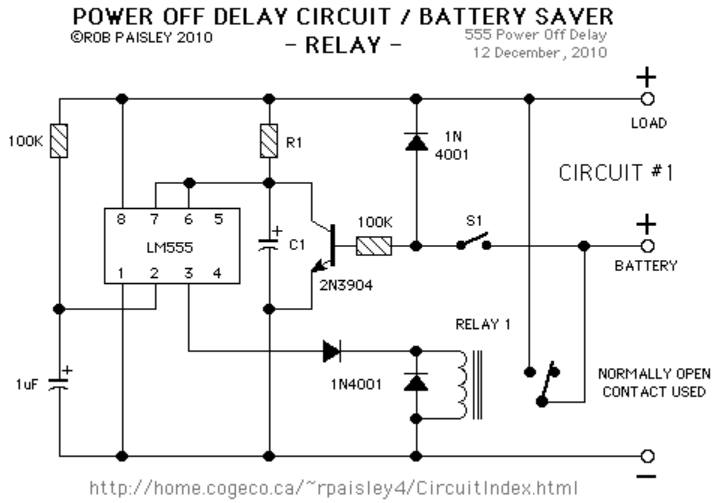
**'N' Steps And Stop Circuit**




## Power OFF Delay Circuits

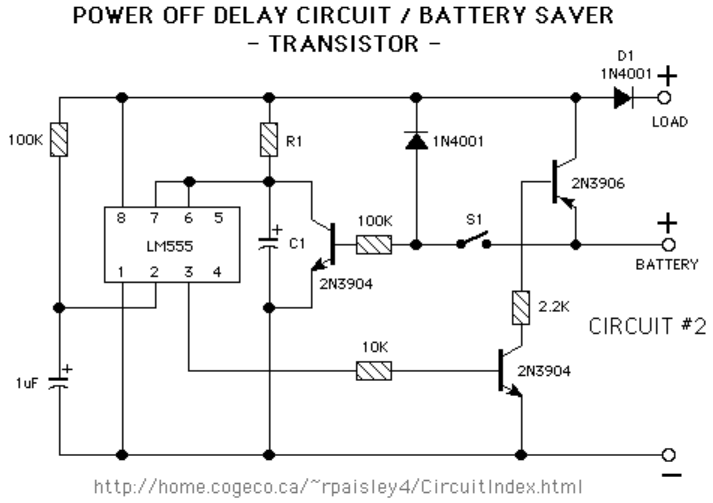
These circuits will delay the removal of power to an external circuit by using mechanical relays or transistors. Other output control devices could also be used.

**Various Power OFF Delay Circuits**




- WHEN S1 IS CLOSED, THE CIRCUIT WILL TURN ON, CLOSE THE RELAY AND SUPPLY POWER TO THE LOAD.
- WHEN S1 IS OPEN, THE 555 TIMER WILL START ITS DELAY AS DETERMINED BY R1 AND C1.
- AT THE END OF THE DELAY TIME, THE RELAY WILL OPEN AND CUT OFF THE POWER TO THE LOAD AND TIMING CIRCUIT.

- AS LONG AS S1 IS CLOSED, THE TIMER'S COUNT WILL REMAIN AT ZERO.
- THE CIRCUIT WILL NOT TRIGGER WHEN POWER IS APPLIED TO THE CIRCUIT.




- WHEN S1 IS CLOSED, THE CIRCUIT WILL TURN ON AND SUPPLY POWER TO THE LOAD.
- WHEN S1 IS OPEN, THE 555 TIMER WILL START ITS DELAY AS DETERMINED BY R1 AND C1.
- AT THE END OF THE DELAY TIME, THE POWER TO THE LOAD AND TIMING CIRCUIT SILL BE CUT OFF.

- AS LONG AS S1 IS CLOSED, THE TIMER'S COUNT WILL REMAIN AT ZERO.
- THE CIRCUIT WILL NOT TRIGGER WHEN POWER IS APPLIED TO THE CIRCUIT.
- D1 IS NEEDED IF THE LOAD HAS LARGE CAPACITORS.

RESET And CONTROL Input Terminal Notes

**Return to the Main Page**

## Please Read Before Using These Circuit Ideas

**The explanations for the circuits on these pages cannot hope to cover every situation on every layout. For this reason be prepared to do some experimenting to get the results you want. This is especially true of circuits such as the "Across Track Infrared Detection" circuits and any other circuit that relies on other than direct electronic inputs, such as switches.**

**If you use any of these circuit ideas, ask your parts supplier for a copy of the manufacturers data sheets for any components that you have not used before. These sheets contain a wealth of data and circuit design information that no electronic or print article could approach and will save time and perhaps damage to the components themselves. These data sheets can often be found on the web site of the device manufacturers.**

**Although the circuits are functional, the pages are not meant to be full descriptions of each circuit but rather as guides for adapting them for use by others. If you have any questions or comments please send them to the email address on the Circuit Index page.**

**Return to the Main Page**

09 July, 2011